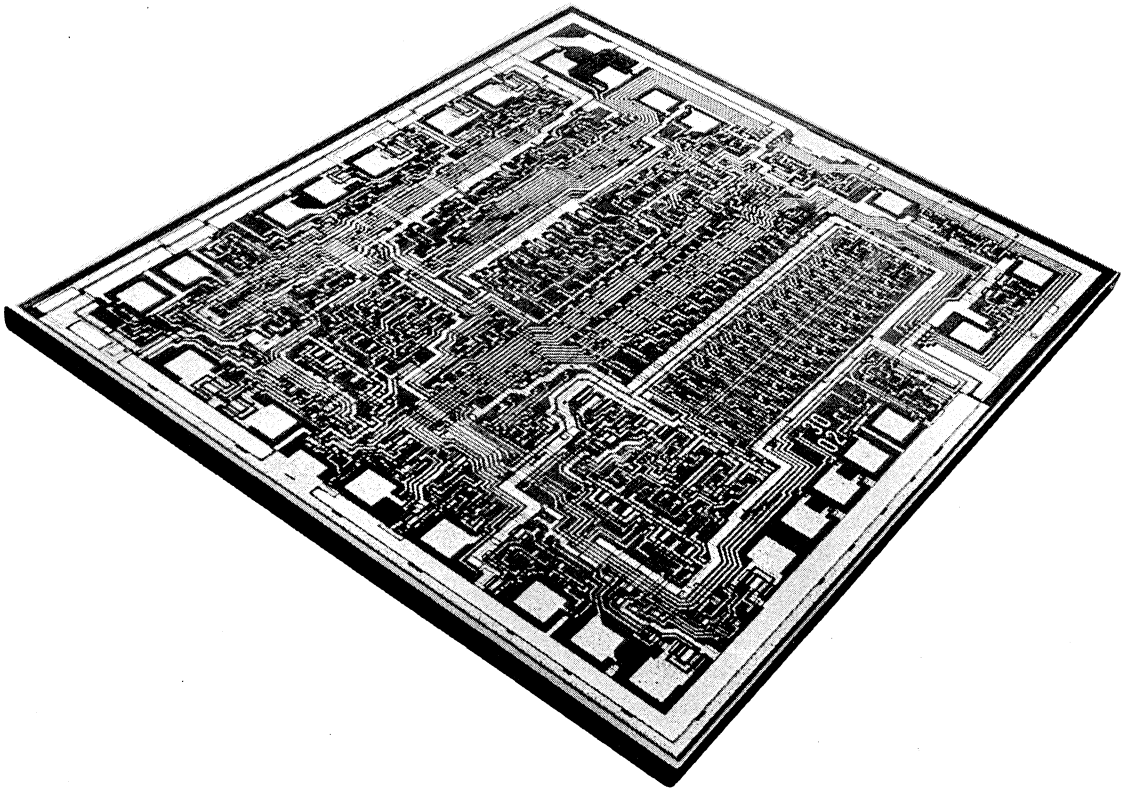


SERIES 3000 BIPOLAR MICROCOMPUTER SYSTEM



SERIES 3000

BIPOLAR MICROCOMPUTER SYSTEM

TYPE	DESCRIPTION	PAGE NO.
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3002	Central Processing Element	9-13
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Since its introduction, the Series 3000 family of computing elements has found acceptance in a wide range of high performance applications from disk controllers to airborne central processors. The Series 3000 offers the flexibility, performance, and system integration necessary for an effective system solution for both high speed controllers and central processors.

The unique multiple bus structure of the 3002 Central Processing Element (CPE) eliminates the need for input data multiplexers or output latches. It also allows the designer to tailor the CPE's to suit his particular processing requirements. The 3001 Microprogram Control Unit (MCU) addresses up to 512 words of microprogram memory and controls both conditional and unconditional jumps within microprogram memory.

The entire component family has been designed to interconnect directly, minimizing the need for ancillary circuitry. It is available in commercial and military temperature range versions. In addition to the components, Intel has also developed a comprehensive support system to assist the user in writing microprograms, debugging hardware and microcode, and programming PROMs for both prototype and production systems.

Thus, with a complete family of components and a powerful development system, Intel provides a Total System Solution, from development to production.



3001

MICROPROGRAM CONTROL UNIT

The INTEL® 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register.

- Selection of the next microinstruction based on the contents of the microprogram address register.

- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.

- Saving and testing of carry output data from the central processor (CP) array.

- Control of carry/shift input data to the CP array.

- Control of microprogram interrupts.

High Performance — 85 ns Cycle Time

TTL and DTL Compatible

Fully Buffered Three-State and Open Collector Outputs

Direct Addressing of Standard Bipolar PROM or ROM

512 Microinstruction Addressability

Advanced Organization

- 9-Bit Microprogram Address Register and Bus

- 4-Bit Program Latch

- Two Flag Registers

Eleven Address Control Functions

- Three Jump and Test Latch Functions

- 16-way Jump and Test Instruction Bus Function

Eight Flag Control Functions

- Four Flag Input Functions

- Four Flag Output Functions

40 Pin DIP

PACKAGE CONFIGURATION

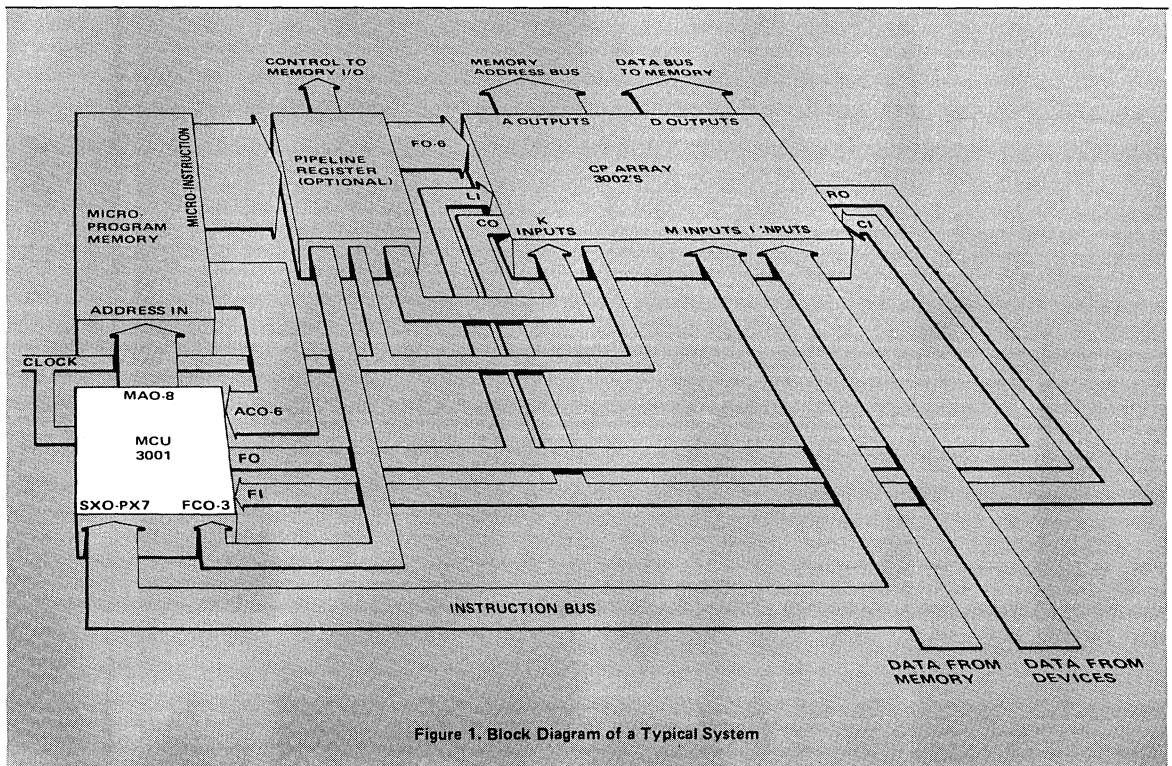
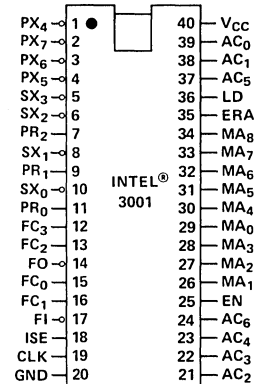


Figure 1. Block Diagram of a Typical System

SERIES
3000

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE ⁽¹⁾
1-4	PX ₄ -PX ₇	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	active LOW
5, 6, 8, 10	SX ₀ -SX ₃	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	active LOW
7, 9, 11	PR ₀ -PR ₂	PR-Latch Outputs The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	open collector
12, 13, 15, 16	FC ₀ -FC ₃	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	
14	FO	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	active LOW three-state
17	FI	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: the flag input data is saved in the F-latch when the clock input (CLK) is low.	active LOW
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description, page 6). It can be used to provide the strobe signal required by the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits.	
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC ₀ -AC ₆	Next Address Control Function Inputs All jump functions are selected by these control lines.	
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA ₀ -MA ₃	Microprogram Column Address Outputs	three-state
30-34	MA ₄ -MA ₈	Microprogram Row Address Outputs	three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used with the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits to facilitate the implementation of priority interrupt systems.	
36	LD	Microprogram Address Load Input When in the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	
40	VCC	+5 Volt Supply	

NOTE:

(1) Active HIGH unless otherwise specified.

LOGICAL DESCRIPTION

The MCU performs two major control functions. First, it controls the sequence in which microinstructions are fetched from the microprogram memory. For this purpose, the MCU contains a microprogram address register and the associated logic for selecting the next microinstruction address. The second function of the MCU is the control of the two flag flip-flops that are included for interaction with the carry input and carry output logic of the CP array. The logical organization of the MCU is shown in Figure 2.

NEXT ADDRESS LOGIC

The next address logic of the MCU provides a set of conditional and unconditional address control functions. These address control functions are used to implement a jump or jump/test operation as part of every microinstruction. That is to say, each microinstruction typically contains a jump operation field that specifies the address control function, and hence, the next microprogram address.

In order to minimize the pin count of the MCU, and reduce the complexity of the next address logic, the microprogram address space is organized as a two dimensional array or matrix. Each microprogram address corresponds to a unit of the matrix at a particular row and column location. Thus, the 9-bit microprogram address is treated as specifying not one, but two addresses — the row address in the upper five bits and the column address in the lower four bits. The address matrix can therefore contain, at most, 32 row addresses and 16 column addresses for a total of 512 microinstructions.

The next address logic of the MCU makes extensive use of this two component addressing scheme. For example, from a particular row or column address, it is possible to jump unconditionally in one operation anywhere in that row or column. It is not possible, however, to jump anywhere in the address matrix. In fact, for a given location in the matrix, there is a fixed subset of microprogram addresses that may be selected as the next address. These

possible jump target addresses are referred to as a jump set. Each type of MCU address control (jump) function has a jump set associated with it. Appendix C illustrates the jump set for each function.

FLAG LOGIC

The flag logic of the MCU provides a set of functions for saving the current value of the carry output of the CP array and for controlling the value of the carry input to the CP array. These two distinct flag control functions are called flag input functions and flag output functions.

The flag logic is comprised of two flip-flops, designated the C-flag and the Z-flag, along with a simple latch, called the F-latch, that indicates the current state of the carry output line of the CP array. The flag logic is used in conjunction with the carry and shift logic of the CP array to implement a variety of shift/rotate and arithmetic functions.

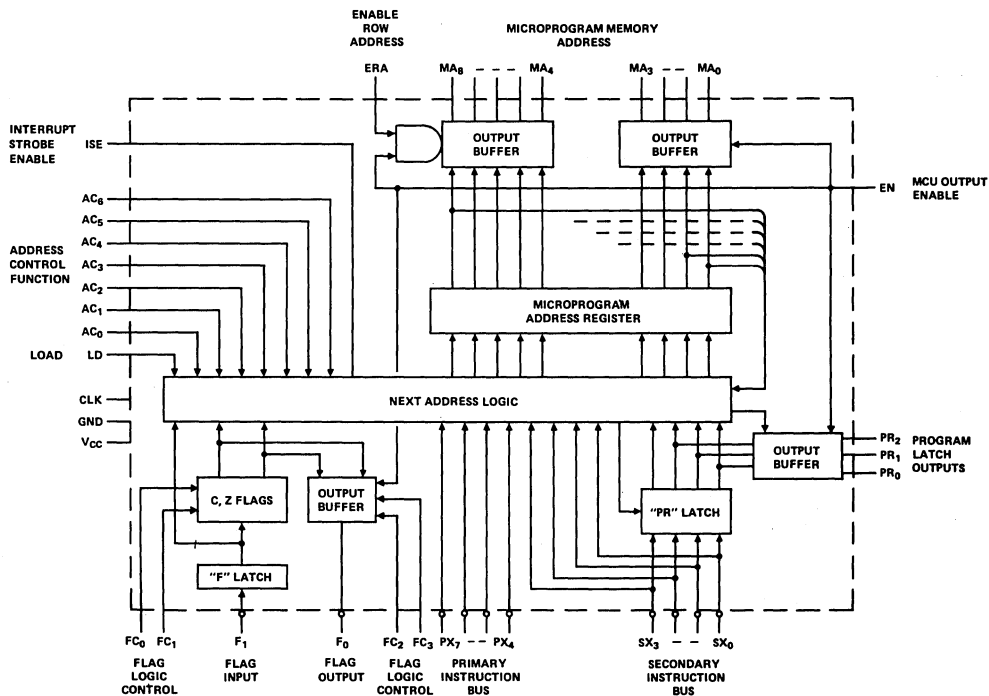
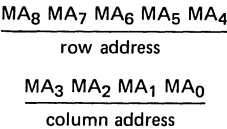


Figure 2. 3001 Block Diagram

FUNCTIONAL DESCRIPTION

ADDRESS CONTROL FUNCTIONS

The address control functions of the MCU are selected by the seven input lines designated AC₀-AC₆. On the rising edge of the clock, the 9-bit microprogram address generated by the next address logic is loaded into the microprogram address register. The next microprogram address is delivered to the microprogram memory via the nine output lines designated MA₀-MA₈. The microprogram address outputs are organized into row and column addresses as:



Each address control function is specified by a unique encoding of the data on the function input lines. From three to five bits of the data specify the particular function while the remaining bits are used to select part of either the row or column address desired. Function code formats are given in Appendix A, "Address Control Function Summary."

The following is a detailed description of each of the eleven address control functions. The symbols shown below are used throughout the description to specify row and column addresses.

Symbol	Meaning
row _n	5-bit next row address where n is the decimal row address.
col _n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

Mnemonic	Function Description
JCC	Jump in current column. AC ₀ -AC ₄ are used to select 1 of 32 row addresses in the current column, specified by

MA₀-MA₃, as the next address

JZR	Jump to zero row. AC ₀ -AC ₃ are used to select 1 of 16 column addresses in row ₀ , as the next address.
JCR	Jump in current row. AC ₀ -AC ₃ are used to select 1 of 16 addresses in the current row, specified by MA ₄ -MA ₈ , as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ -MA ₈ , as the next row address. The current column is specified by MA ₀ -MA ₃ . The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JFL	Jump/test F-Latch. AC ₀ -AC ₃ are used to select 1 of 16 row addresses in the current row group, specified by MA ₈ , as the next row address. If the current column group, specified by MA ₃ , is col ₀ -col ₇ , the F-latch is used to select col ₂ or col ₃ as the next column address. If MA ₃ specifies column group col ₈ -col ₁₅ , the F-latch is used to select col ₁₀ or col ₁₁ as the next column address.
JCF	Jump/test C-flag. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current

row group, specified by MA₇ and MA₈, as the next row address. If the current column group specified by MA₃ is col₀-col₇, the C-flag is used to select col₂ or col₃ as the next column address. If MA₃ specifies column group col₈-col₁₅, the C-flag is used to select col₁₀ or col₁₁ as the next column address.

JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.
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PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX₄-PX₇), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JPR	Jump/test PR-latch. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test leftmost PR-latch bits. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₂ and PR ₃ are used to

FUNCTIONAL DESCRIPTION (con't)

	select 1 of 4 possible column addresses in col ₄ through col ₇ as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC ₀ and AC ₁ are used to select 1 of 4 high-order row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₀ and PR ₁ are used to select 1 of 4 possible column addresses in col ₁₂ through col ₁₅ as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC ₀ and AC ₁ are used to select 1 of 4 row addresses in the current row group, specified by MA ₆ –MA ₈ , as the next row address. PX ₄ –PX ₇ are used to select 1 of 16 possible column addresses as the next column address. SX ₀ –SX ₃ data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC₀–FC₃. Function code formats are given in Appendix B, "Flag Control Function Summary."

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Mnemonic	Function Description
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

Mnemonic	Function Description
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

LOAD AND INTERRUPT STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the data on the primary and secondary instruction busses, PX₄–PX₇ and SX₀–SX₃, is loaded into the microprogram address register. PX₄–PX₇ are loaded into MA₀–MA₃ and SX₀–SX₃ are loaded into MA₄–MA₇. The high-order bit of the microprogram address register MA₈ is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The interrupt strobe enable of the MCU is available on the output line designated ISE. The line is placed in the active high state whenever a JZR to col₁₅ is selected as the address control function. Customarily, the start of a macroinstruction fetch sequence is situated at row₀ and col₁₅ so that the INTEL 3214 Priority Interrupt Control Unit may be enabled at the beginning of the fetch/execute cycle. The priority interrupt control unit may respond to the interrupt by pulling the enable row address (ERA) input line down to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC₀–AC₆. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$$T_A = 0^\circ\text{C to } 70^\circ\text{C} \quad V_{CC} = 5.0\text{V} \pm 5\%$$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT	CONDITIONS
V _C	Input Clamp Voltage (All Input Pins)		-0.8	-1.0	V	I _C = -5 mA
I _F	Input Load Current:					
	CLK Input		-0.075	-0.75	mA	V _F = 0.45V
	EN Input		-0.05	-0.50	mA	
	All Other Inputs		-0.025	-0.25	mA	
I _R	Input Leakage Current:					
	CLK			120	μA	V _R = 5.25V
	EN Input			80	μA	
	All Other Inputs			40	μA	
V _{IL}	Input Low Voltage			0.8	V	V _{CC} = 5.0V
V _{IH}	Input High Voltage	2.0			V	
I _{CC}	Power Supply Current ⁽²⁾		170	240	mA	
V _{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I _{OL} = 10 mA
V _{OH}	Output High Voltage (MA ₀ -MA ₈ , ISE, FO)	2.4	3.0		V	I _{OH} = -1 mA
I _{OS}	Output Short Circuit Current (MA ₀ -MA ₈ , ISE, FO)	-15	-28	-60	mA	V _{CC} = 5.0V
I _{O (off)}	Off-State Output Current:					
	MA ₀ -MA ₈ , FO			-100	μA	V _O = 0.45V
	MA ₀ -MA ₈ , FO, PR ₀ -PR ₂			100	μA	V _O = 5.25V

NOTES:

- (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{CY}	Cycle Time ⁽²⁾	85	60		ns
t_{WP}	Clock Pulse Width	30	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC ₀ -AC ₆	10	0		ns
t_{SK}	FC ₀ , FC ₁	0			ns
t_{SX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC ₀ -AC ₆	5	0		ns
t_{HK}	FC ₀ , FC ₁	0			ns
t_{HX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	20	5		ns
t_{HI}	FI	20	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA ₀ -MA ₈ , FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC ₂ and FC ₃ to Flag Out (FO)		16	30	ns
t_{FO}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Latch Outputs (PR ₀ -PR ₂)		26	40	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA ₀ -MA ₈ , FO, PR ₀ -PR ₂)		21	32	ns
t_{FI}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Interrupt Strobe Enable Output (ISE)		24	40	ns

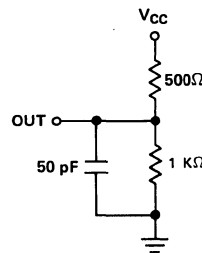
NOTE:(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$ **TEST CONDITIONS:**

Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5 ns between 1 volt and 2 volts.

Output load of 10 mA and 50 pF.

Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:**CAPACITANCE⁽²⁾** $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +160°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.2	V	$I_C = -5\text{ mA}$
I_F	Input Load Current:					$V_F = 0.45\text{V}$
	CLK Input		−75	−750	μA	
	EN Input		−50	−500	μA	
	All Other Inputs		−25	−250	μA	
I_R	Input Leakage Current:					$V_R = 5.5\text{V}$
	CLK			120	μA	
	EN Input			80	μA	
	All Other Inputs			40	μA	
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current ⁽²⁾		170	250	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output High Voltage (MA_0 – MA_8 , ISE, FO)	2.4	3.0		V	$I_{OH} = -1\text{ mA}$
I_{OS}	Output Short Circuit Current (MA_0 – MA_8 , ISE, FO)	−15	−28	−60	mA	$V_{CC} = 5.0\text{V}$
$I_{O(off)}$	Off-State Output Current:					
	MA_0 – MA_8 , FO			−100	μA	$V_O = 0.45\text{V}$
	MA_0 – MA_8 , FO, PR_0 – PR_2			100	μA	$V_O = 5.5\text{V}$

NOTES:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{CY}	Cycle Time ⁽²⁾	95	60		ns
t_{WP}	Clock Pulse Width	40	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC ₀ -AC ₆	10	0		ns
t_{SK}	FC ₀ , FC ₁	0			ns
t_{SX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC ₀ -AC ₆	5	0		ns
t_{HK}	FC ₀ , FC ₁	0			ns
t_{HX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	25	5		ns
t_{HI}	FI	22	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA ₀ -MA ₈ , FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC ₂ and FC ₃ to Flag Out (FO)		16	50	ns
t_{FO}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Latch Outputs (PR ₀ -PR ₂)		26	50	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA ₀ -MA ₈ , FO, PR ₀ -PR ₂)		21	35	ns
t_{FI}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Interrupt Strobe Enable Output (ISE)		24	40	ns

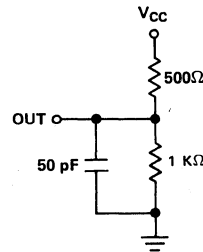
NOTE:(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$ **TEST CONDITIONS:**

Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5 ns between 1 volt and 2 volts.

Output load of 10 mA and 50 pF.

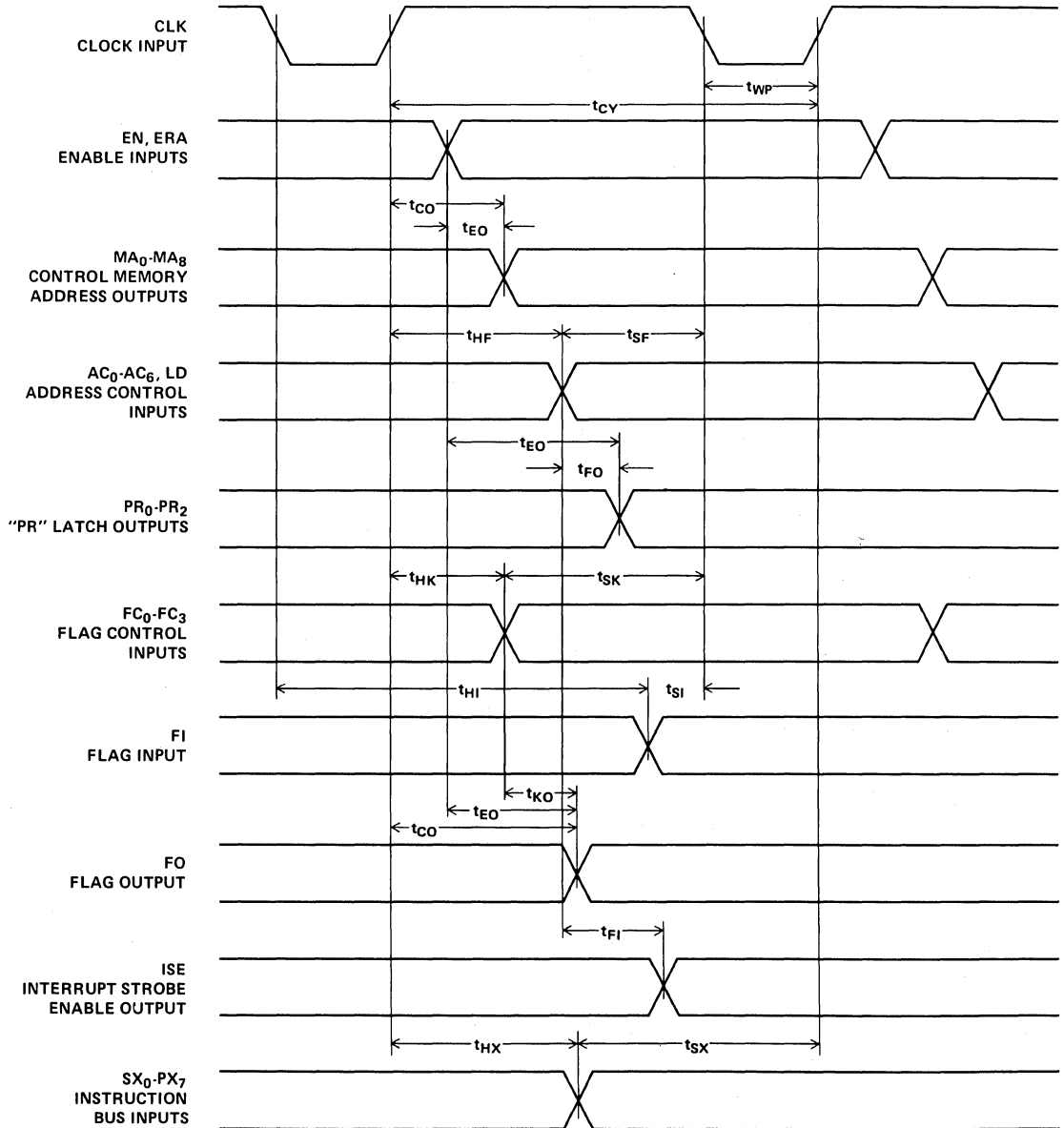
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:**CAPACITANCE ⁽²⁾ $T_A = 25^\circ\text{C}$**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

3001 WAVEFORMS





3002

CENTRAL PROCESSING ELEMENT

The INTEL® 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N, it is simply necessary to connect an array of N/2 CPE's together. When wired together in such an array, a set of CPE's provide the following capabilities:

- 2's complement arithmetic
- Logical AND, OR, NOT and exclusive-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

High Performance — 100 ns Cycle Time

TTL and DTL Compatible

N-Bit Word Expandable Multi-Bus Organization

- 3 Input Data Busses
- 2 Three-State Fully Buffered Output Data Busses

11 General Purpose Registers

Full Function Accumulator

Independent Memory Address Register

Cascade Outputs for Full Carry Look-Ahead

Versatile Functional Capability

- 8 Function Groups
- Over 40 Useful Functions
- Zero Detect and Bit Test

Single Clock

28 Pin DIP

PACKAGE CONFIGURATION

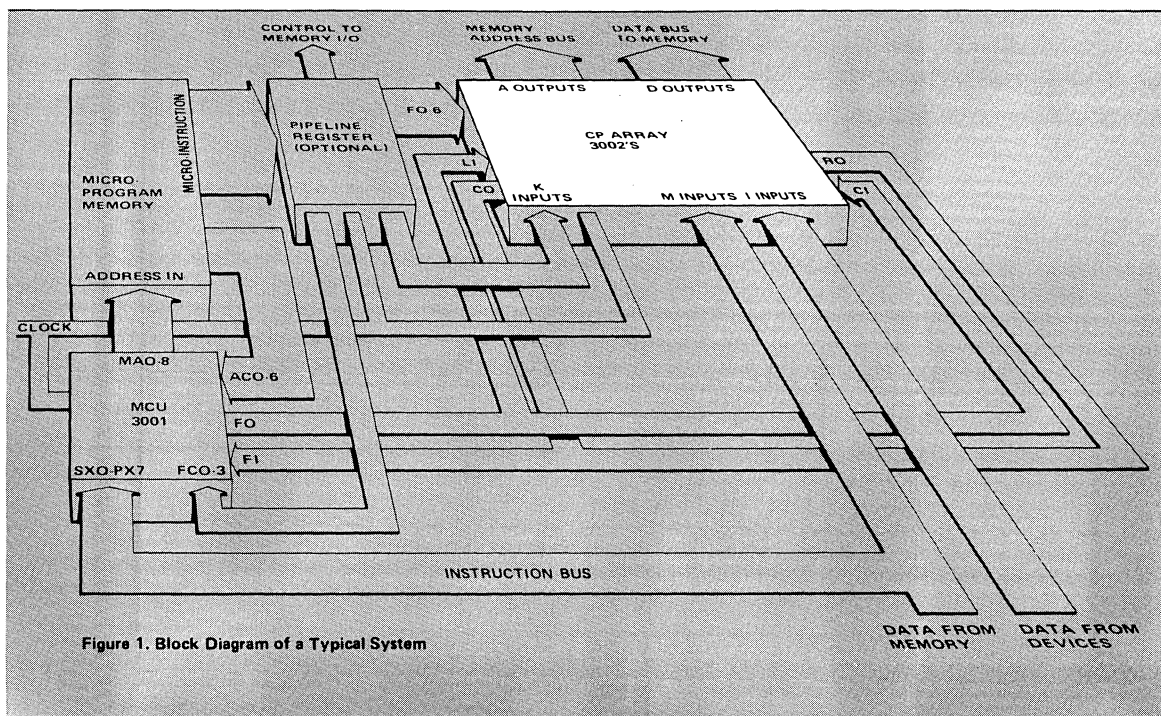
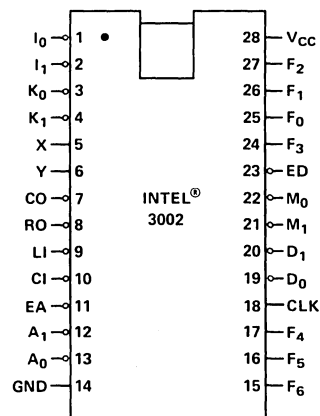


Figure 1. Block Diagram of a Typical System

SERIES
3000

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE ⁽¹⁾
1, 2	I ₀ -I ₁	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3, 4	K ₀ -K ₁	Mask Bus Inputs The mask bus inputs provide a separate input port for the microprogram memory, to allow mask or constant entry.	Active LOW
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the INTEL 3003 Look-Ahead Carry Generator.	
7	CO	Ripple Carry Output The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	RO	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	LI	Shift Right Input	Active LOW
10	CI	Carry Input	Active LOW
11	EA	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A ₀ -A ₁).	Active LOW
12-13	A ₀ -A ₁	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15-17, 24-27,	F ₀ -F ₆	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	
18	CLK	Clock Input	
19-20	D ₀ -D ₁	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21-22	M ₀ -M ₁	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	ED	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D ₀ -D ₁)	Active LOW
28	V _{CC}	+5 Volt Supply	

NOTE:

1. Active HIGH, unless otherwise specified.

LOGICAL DESCRIPTION

The CPE provides the arithmetic, logic and register functions of a 2-bit wide slice through a microprogrammed central processor. Data from external sources such as main memory, is brought into the CPE on one of the three separate input busses. Data being sent out of the CPE to external devices is carried on either of the two output busses. Within the CPE, data is stored in one of eleven scratchpad registers or in the accumulator. Data from the input busses, the registers, or the accumulator is available to the arithmetic/logic section (ALS) under the control of two internal multiplexers. Additional inputs and outputs are included for carry propagation, shifting, and micro-function selection. The complete logical organization of the CPE is shown below.

MICRO-FUNCTION BUS AND DECODER

The seven micro-function bus input lines of the CPE, designated F_0 - F_6 , are decoded internally to select the ALS function, generate the scratchpad address, and control the A and B multiplexers.

M-BUS AND I-BUS INPUTS

The M-bus inputs are arranged to bring data from an external main memory into the CPE. Data on the M-bus is multiplexed internally for input to the ALS.

The I-bus inputs are arranged to bring data from an external I/O system into the CPE. Data on the I-bus is also multiplexed internally, although independently of the M-bus, for input to the ALS. Separation of the two busses permits a relatively lightly loaded memory bus even though a large number of I/O devices are connected to the I-bus. Alternatively, the I-bus may be wired to perform a multiple bit shift (e.g., a byte exchange) by connecting it to one of the output busses. In this case, I/O device data is gated externally onto the M-bus.

SCRATCHPAD

The scratchpad contains eleven registers designated R_0 through R_9 and T. The output of the scratchpad is multiplexed internally for input to ALS. The ALS output is returned for input into the scratchpad.

ACCUMULATOR AND D-BUS

An independent register called the accumulator (AC) is available for storing the result of an ALS operation. The output of the accumulator is multiplexed internally for input back to the

ALS and is also available via a three-state output buffer on the D-bus outputs. Conventional usage of the D-bus is for data being sent to the external main memory or to external I/O devices.

A AND B MULTIPLEXERS

The A and B multiplexers select the two inputs to the ALS specified on the micro-function bus. Inputs to the A-multiplexer include the M-bus, the scratchpad, and the accumulator. The B-multiplexer selects either the I-bus, the accumulator, or the K-bus. The selected B-multiplexer input is always logically ANDed with the data on the K-bus (see below) to provide a flexible masking and bit testing capability.

ALS AND K-BUS

The ALS is capable of a variety of arithmetic and logic operations, including 2's complement addition, incrementing, and decrementing, plus logical AND, inclusive-OR, exclusive-NOR, and logical complement. The result of an ALS operation may be stored in the accumulator or one of the scratchpad registers. Separate left input and right output lines, designated LI and RO, are available for use in right shift operations. Carry input and carry output lines, designated CI and CO, are provided for normal ripple carry propaga-

tion. CO and RO data are brought out via two alternately enabled tri-state buffers. In addition, standard look ahead carry outputs, designated X and Y, are available for full carry look ahead across any word length.

The ability of the K-bus to mask inputs to the ALS greatly increases the versatility of the CPE. During non-arithmetic operations in which carry propagation has no meaning, the carry circuits are used to perform a word-wise inclusive-OR of the bits, masked by the K-bus, from the register or bus selected by the function decoder. Thus, the CPE provides a flexible bit testing capability. The K-bus is also used during arithmetic operations to mask portions of the field being operated upon. An additional function of the K-bus is that of supplying constants to the CPE from the microprogram.

MEMORY ADDRESS REGISTER AND A-BUS

A separate ALS output is also available to the memory address register (MAR) and to the A-bus via a three-state output buffer. Conventional usage of the MAR and A-bus is for sending addresses to an external main memory. The MAR and A-bus may also be used to select an external device when executing I/O operations.

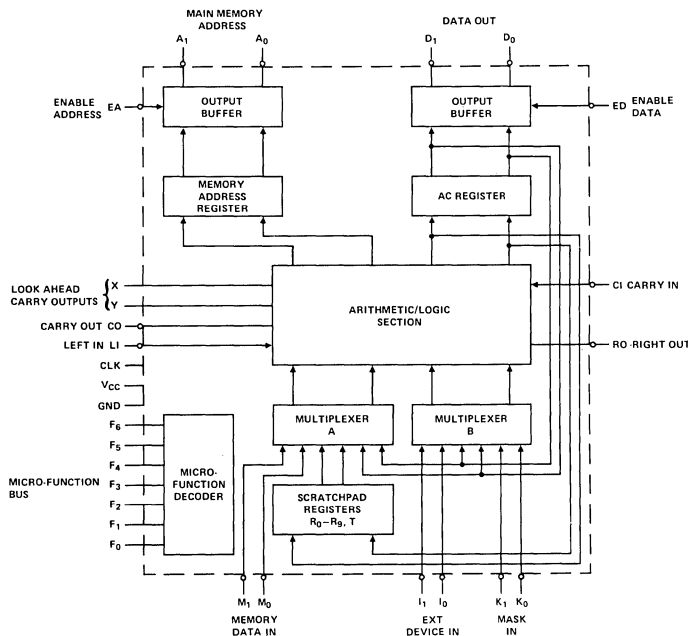


Figure 2. 3002 Block Diagram

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	LIMITS		UNIT	CONDITIONS
			TYP ⁽¹⁾	MAX		
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.0	V	$I_C = -5\text{ mA}$
I_F	Input Load Current:					
	F_0 - F_6 , CLK, K_0 , K_1 , EA, ED		-0.05	-0.25	mA	$V_F = 0.45\text{V}$
	I_0 , I_1 , M_0 , M_1 , LI		-0.85	-1.5	mA	
	CI		-2.3	-4.0	mA	
I_R	Input Leakage Current:					
	F_0 - F_6 , CLK, K_0 , K_1 , EA, ED			40	μA	$V_R = 5.25\text{V}$
	I_0 , I_1 , M_0 , M_1 , LI			60	μA	
	CI			180	μA	
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current ⁽²⁾		145	190	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.3	0.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output High Voltage (All Output Pins)	2.4	3.0		V	$I_{OH} = -1\text{ mA}$
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-25	-60	mA	$V_{CC} = 5.0\text{V}$
$I_{O(off)}$	Off State Output Current			-100	μA	$V_O = 0.45\text{V}$
	A_0 , A_1 , D_0 , D_1 , CO and RO			100	μA	$V_O = 5.25\text{V}$

NOTES:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage

(2) CLK input grounded, other inputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{CY}	Clock Cycle Time ⁽²⁾	100	70		ns
t_{WP}	Clock Pulse Width	33	20		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	60	40		ns
	Data Set-Up Time:				
t_{DS}	$I_0, I_1, M_0, M_1, K_0, K_1$	50	30		ns
t_{SS}	LI, CI	27	13		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	5	-2		ns
t_{DH}	$I_0, I_1, M_0, M_1, K_0, K_1$	5	-4		ns
t_{SH}	LI, CI	15	2		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		37	52	ns
t_{XD}	Any Data Input		29	42	ns
t_{XT}	Trailing Edge of CLK		40	60	ns
t_{XL}	Leading Edge of CLK	20			ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	20			ns
t_{CT}	Trailing Edge of CLK		48	70	ns
t_{CF}	Any Function Input		43	65	ns
t_{CD}	Any Data Input		30	55	ns
t_{CC}	CI (Ripple Carry)		14	25	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK	5	32	50	ns
t_{DE}	Enable Input ED, EA		12	25	ns

NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(2) $t_{CY} = t_{DS} + t_{DL}$.

TEST CONDITIONS:

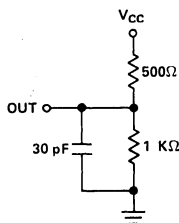
Input pulse amplitude: 2.5 V

Input rise and fall times of 5 ns between 1 and 2 volts.

Output loading is 10 mA and 30 pF.

Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:

CAPACITANCE⁽²⁾ $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:

(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$.

SYMBOL	PARAMETER	MIN	LIMITS		UNIT	CONDITIONS
			TYP ⁽¹⁾	MAX		
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.2	V	$I_C = -5\text{ mA}$
I_F	Input Load Current:					$V_F = 0.45\text{V}$
	F_0 - F_6 , CLK, K_0 , K_1 , EA, ED		-0.05	-0.25	mA	
	I_0 , I_1 , M_0 , M_1 , LI		-0.85	-1.5	mA	
	CI		-2.3	-4.0	mA	
I_R	Input Leakage Current:					$V_R = 5.5\text{V}$
	F_0 - F_6 , CLK, K_0 , K_1 , EA, ED			40	μA	
	I_0 , I_1 , M_0 , M_1 , LI			100	μA	
	CI			250	μA	
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current		145	210	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.3	0.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output High Voltage (All Output Pins)	2.4	3.0		V	$I_{OH} = -1\text{ mA}$
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-25	-60	mA	$V_{CC} = 5.0\text{V}$
$I_{O(\text{off})}$	Off State Output Current			-100	μA	$V_O = 0.45\text{V}$
	A_0 , A_1 , D_0 , D_1 , CO and RO			100	μA	$V_O = 5.5\text{V}$

NOTES:

- (1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage
 (2) CLK input grounded, other inputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$.

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{CY}	Clock Cycle Time ^[2]	120	70		ns
t_{WP}	Clock Pulse Width	42	20		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	70	40		ns
	Data Set-Up Time:				
t_{DS}	$I_0, I_1, M_0, M_1, K_0, K_1$	60	30		ns
t_{SS}	$L1, C1$	30	13		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	5	-2		ns
t_{DH}	$I_0, I_1, M_0, M_1, K_0, K_1$	5	-4		ns
t_{SH}	$L1, C1$	15	2		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		37	65	ns
t_{XD}	Any Data Input		29	55	ns
t_{XT}	Trailing Edge of CLK		40	75	ns
t_{XL}	Leading Edge of CLK	22			ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	22			ns
t_{CT}	Trailing Edge of CLK		48	85	ns
t_{CF}	Any Function Input		43	75	ns
t_{CD}	Any Data Input		30	65	ns
t_{CC}	$C1$ (Ripple Carry)		14	30	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK	5	32	60	ns
t_{DE}	Enable Input ED, EA		12	35	ns

NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(2) $t_{CY} = t_{DS} + t_{DL}$

TEST CONDITIONS:

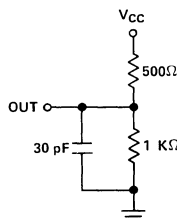
Input pulse amplitude: 2.5 V

Input rise and fall times of 5 ns between 1 and 2 volts.

Output loading is 10 mA and 30 pF.

Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:

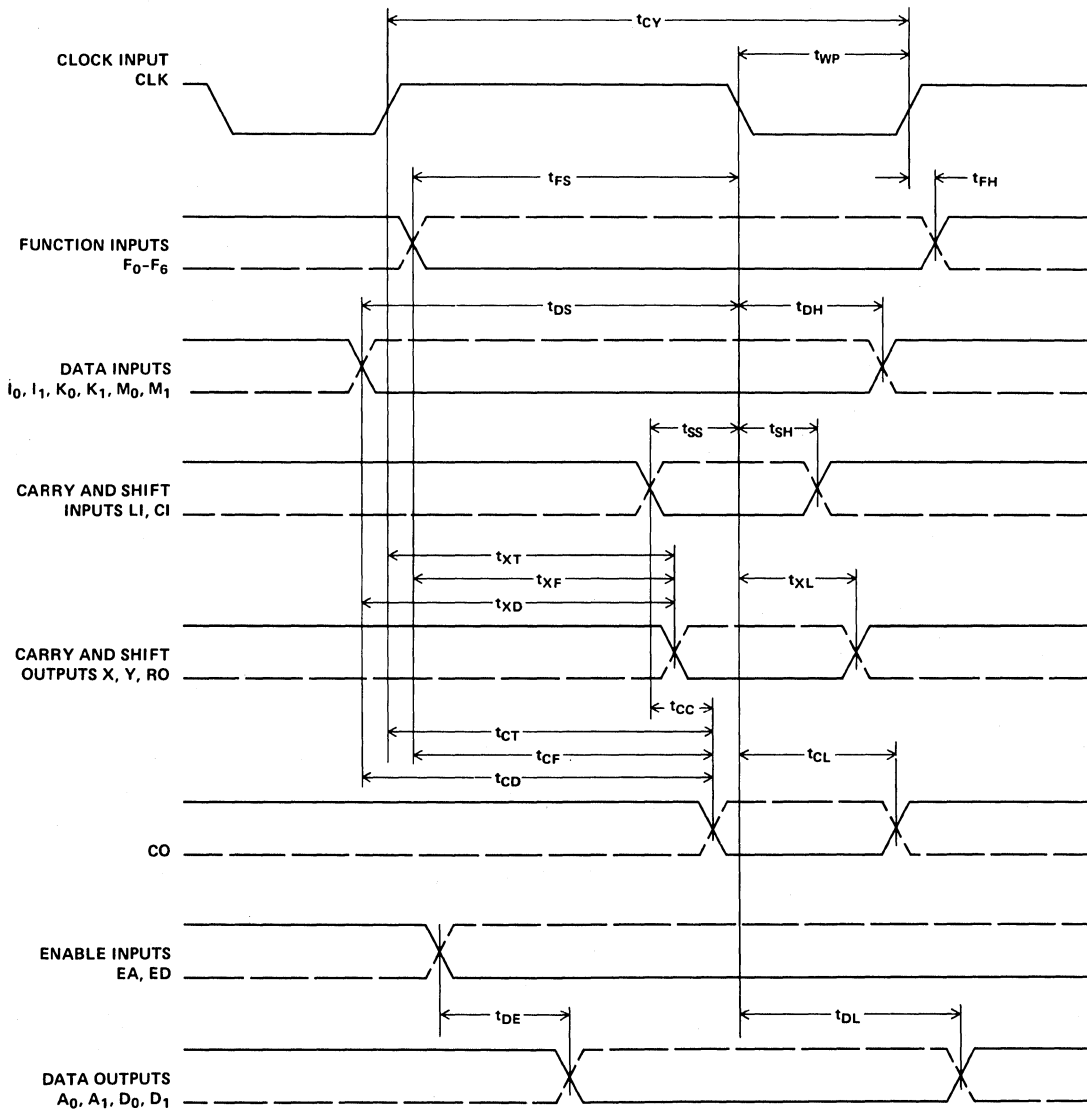
CAPACITANCE⁽²⁾ $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:

(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.

3002 WAVEFORMS





3003

LOOK-AHEAD CARRY GENERATOR

The INTEL® 3003 Look-Ahead Carry Generator (LCG) is a high speed circuit capable of anticipating a carry across a full 16-bit 3002 Central Processing Array. When used with a larger 3002 CP Array multiple 3003 carry generators provide high speed carry look-ahead capability for any word length.

The LCG accepts eight pairs of active high cascade inputs (X,Y) and an active low carry input and generates active low carries for up to eight groups of binary adders.

High Performance — 10 ns typical propagation delay

Compatible with INTEL 3001 MCU and 3002 CPE

DTL and TTL compatible

Full look-ahead across 8 adders

Low voltage diode input clamp

Expandable

28-pin DIP

PACKAGE CONFIGURATION

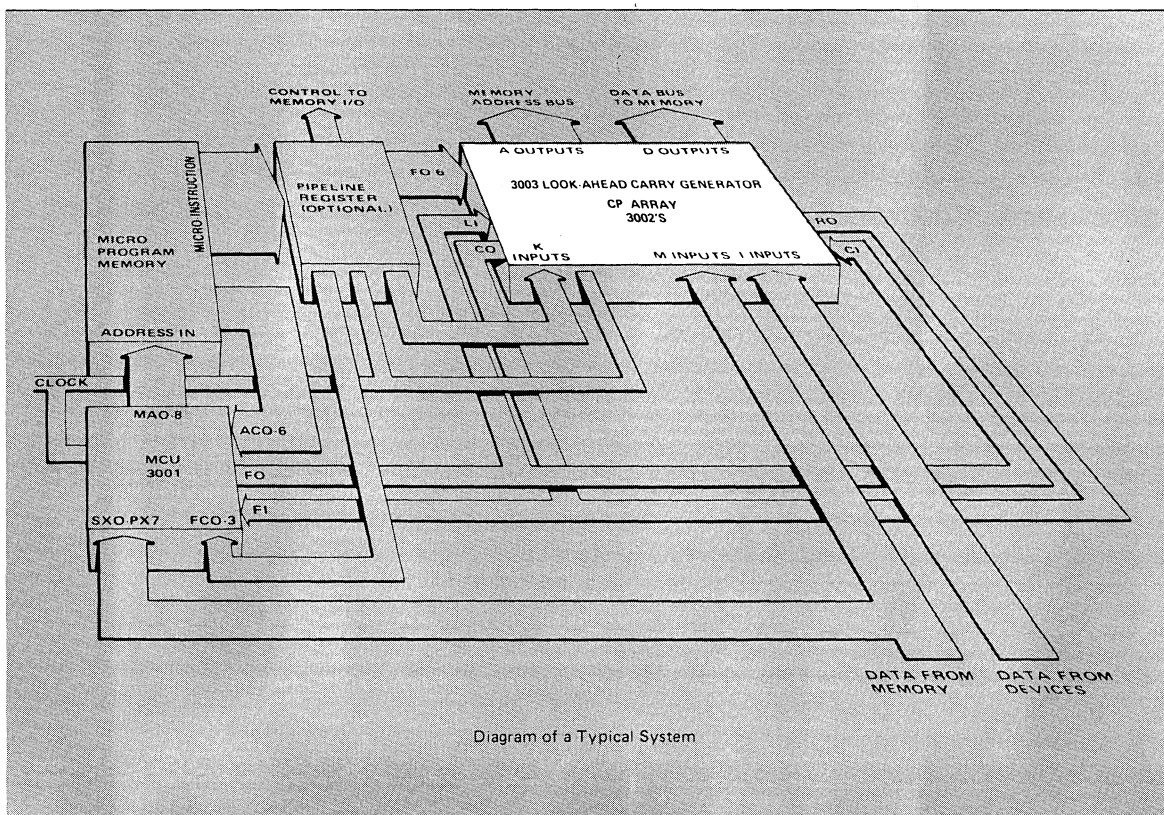
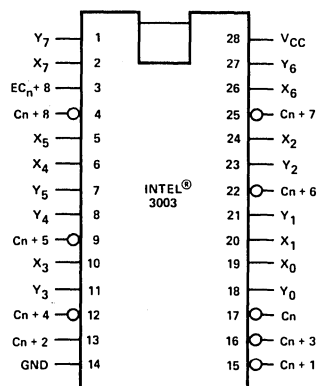


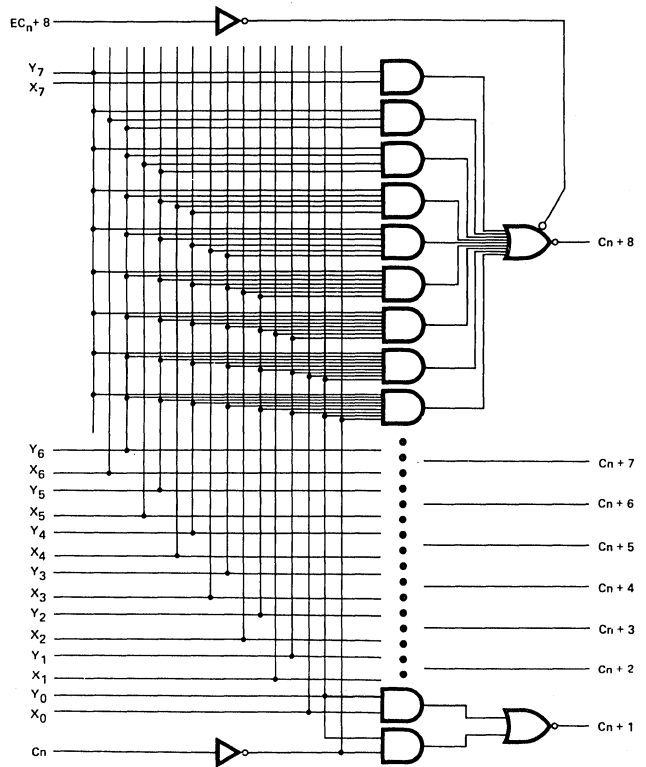
Diagram of a Typical System

SERIES
3000

LOGIC DIAGRAM

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1,7,8,11 18,21,23 27	Y_0-Y_7	Standard carry look-ahead inputs	Active HIGH
2,5,6,10 19,20,24 26	X_0-X_7	Standard carry look-ahead inputs	Active HIGH
17	C_n	Carry input	Active LOW
4,9,12 13,15,16	$C_{n+1}-$ C_{n+8}	Carry outputs	Active LOW
3	EC_{n+8}	C_{n+8} carry output enable	Active HIGH
28	V_{CC}	+5 volt supply	
14	GND	Ground	



3003 LOGIC EQUATIONS

The 3003 Look-Ahead Generator is implemented in a compatible form for direct connection to the 3001 MCU and 3002 CPE. Logic equations for the 3003 are:

$$\overline{C_n + 1} = Y_0 X_0 + Y_0 \overline{C_n}$$

$$\overline{C_n + 2} = Y_1 X_1 + Y_1 Y_0 X_0 + Y_1 Y_0 \overline{C_n}$$

$$\overline{C_n + 3} = Y_2 X_2 + Y_2 Y_1 X_1 + Y_2 Y_1 Y_0 X_0 + Y_2 Y_1 Y_0 \overline{C_n}$$

$$\overline{C_n + 4} = Y_3 X_3 + Y_3 Y_2 X_2 + Y_3 Y_2 Y_1 X_1 + Y_3 Y_2 Y_1 Y_0 X_0 + Y_3 Y_2 Y_1 Y_0 \overline{C_n}$$

$$\overline{C_n + 5} = Y_4 X_4 + Y_4 Y_3 X_3 + Y_4 Y_3 Y_2 X_2 + Y_4 Y_3 Y_2 Y_1 X_1 + Y_4 Y_3 Y_2 Y_1 Y_0 X_0 + Y_4 Y_3 Y_2 Y_1 Y_0 \overline{C_n}$$

$$\overline{C_n + 6} = Y_5 X_5 + Y_5 Y_4 X_4 + Y_5 Y_4 Y_3 X_3 + Y_5 Y_4 Y_3 Y_2 X_2 + Y_5 Y_4 Y_3 Y_2 Y_1 X_1 + Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 X_0 + Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 \overline{C_n}$$

$$\overline{C_n + 7} = Y_6 X_6 + Y_6 Y_5 X_5 + Y_6 Y_5 Y_4 X_4 + Y_6 Y_5 Y_4 Y_3 X_3 + Y_6 Y_5 Y_4 Y_3 Y_2 X_2 + Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 X_1 + Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 X_0 + Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 \overline{C_n}$$

$$\overline{C_n + 8} = \text{High Impedance State when } EC_{n+8} \text{ Low}$$

$$\overline{C_n + 8} = Y_7 X_7 + Y_7 Y_6 X_6 + Y_7 Y_6 Y_5 X_5 + Y_7 Y_6 Y_5 Y_4 X_4 + Y_7 Y_6 Y_5 Y_4 Y_3 X_3 + Y_7 Y_6 Y_5 Y_4 Y_3 Y_2 X_2 + Y_7 Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 X_1 + Y_7 Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 X_0 + Y_7 Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 \overline{C_n} \text{ when } EC_{n+8} \text{ high}$$

D.C. AND OPERATING CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Current	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$.

SYMBOL	PARAMETER	MIN.	TYP. ⁽¹⁾	MAX.	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.2	V	$I_C = -5\text{ mA}$
I_F	Input Load Current: X ₆ , X ₇ , C _n , EC _n +8 Y ₇ , X ₀ -X ₅ , Y ₀ -Y ₆		-0.07 -0.200 -0.6	-0.25 -0.500 -1.5	mA mA mA	$V_F = 0.45\text{V}$
I_R	Input Leakage Current: C _n and EC _n + 8 All Other Inputs			40 100	μA μA	$V_{CC} = 5.25\text{V}$, $V_R = 5.5\text{V}$
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.1			V	$V_{CC} = 5.0\text{V}$
I_{CC}	Power Supply Current		80	130	mA	All Y and EC _n + 8 high, All X and C _n low
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	$I_{OL} = 4\text{ mA}$
V_{OH}	Output High Voltage (All Output Pins)	2.4	3		V	$I_{OH} = -1\text{ mA}$
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-40	-65	mA	$V_{CC} = 5\text{V}$
$I_{O(off)}$	Off-State Output Current (C _n + 8)			-100 +100	μA μA	$V_O = 0.45\text{V}$ $V_O = 5.5\text{V}$

NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

A.C. CHARACTERISTICS

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm 10\%$

SYMBOL	PARAMETER	MIN.	TYP. ⁽¹⁾	MAX.	UNIT
t_{XC}	X, Y to Outputs	3	10	25	ns
t_{CC}	Carry In to Outputs		13	40	ns
t_{EN}	Enable Time, C _n + 8		20	50	ns

NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

D.C. AND OPERATING CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Current	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

$$T_A = 0^\circ\text{C to } 70^\circ\text{C} \quad V_{CC} = 5.0\text{V} \pm 5\%$$

SYMBOL	PARAMETER	MIN.	TYP. ⁽¹⁾	MAX.	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.0	V	$I_C = -5 \text{ mA}$
I_F	Input Load Current: $X_8, X_7, C_n, EC_n + 8$ $Y_7, X_0, X_5,$ Y_0, Y_6		-0.07	-0.25	mA	$V_F = 0.45\text{V}$
			-0.200	-0.500	mA	
			-0.6	-1.5	mA	
I_R	Input Leakage Current: C_n and $EC_n + 8$ All Other Inputs			40	μA	$V_R = 5.25\text{V}$
				100	μA	
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.0			V	$V_{CC} = 5.0\text{V}$
I_{CC}	Power Supply Current		80	130	mA	All Y and $EC_n + 8$ high, All X and C_n low
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	$I_{OL} = 4 \text{ mA}$
V_{OH}	Output High Voltage (All Output Pins)	2.4	3		V	$I_{OH} = -1 \text{ mA}$
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-40	-65	mA	$V_{CC} = 5\text{V}$
$I_{O(off)}$	Off-State Output Current ($C_n + 8$)			-100	μA	$V_O = 0.45\text{V}$
				+100	μA	$V_O = 5.25\text{V}$

NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

A.C. CHARACTERISTICS

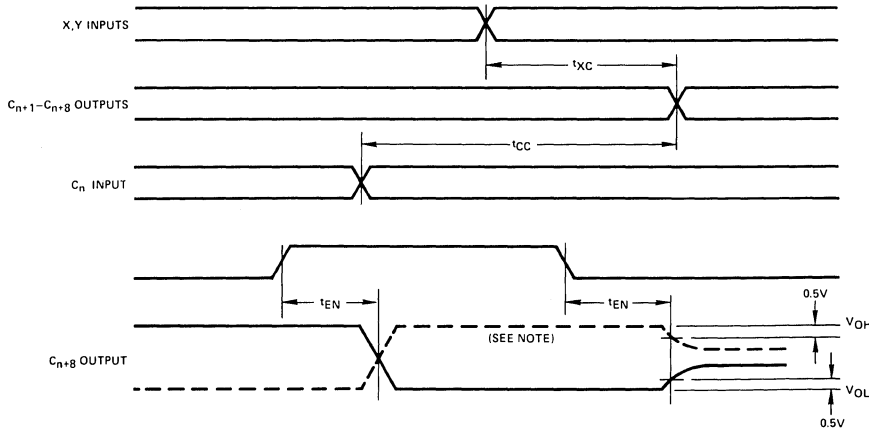
$$T_A = 0^\circ\text{C to } 70^\circ\text{C}, V_{CC} = +5\text{V} \pm 5\%$$

SYMBOL	PARAMETER	MIN.	TYP. ⁽¹⁾	MAX.	UNIT
t_{XC}	X, Y to Outputs	3	10	20	ns
t_{CC}	Carry In to Outputs		13	30	ns
t_{EN}	Enable Time, $C_n + 8$		20	40	ns

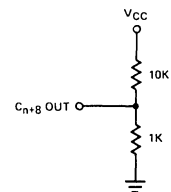
NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

WAVEFORMS



NOTE: ALTERNATE TEST LOAD:

CAPACITANCE⁽²⁾ $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance All inputs		12	20	pF
C_{OUT}	Output Capacitance $C_n + 8$		7	12	pF

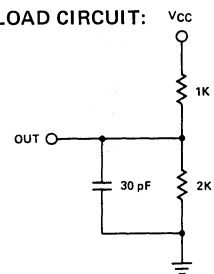
NOTE:

(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 5.0\text{V}$, $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
 Input rise and fall times of 5 ns between 1 and 2 volts.
 Output loading is 5 mA and 30 pF.
 Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:





3212

MULTI-MODE LATCH BUFFER

The INTEL® 3212 Multi-Mode Latch Buffer is a versatile 8-bit latch with three-state output buffers and built-in device select logic. It also contains an independent service request flip-flop for the generation of central processor interrupts. Because of its multi-mode capabilities, one or more 3212's can be used to implement many types of interface and support systems for Series 3000 computing elements including:

- Simple data latches
- Gated data buffers
- Multiplexers
- Bi-directional bus drivers
- Interrupting input/output ports

High Performance — 50 ns Write Cycle Time

Low Input Load Current — 250 μ A Maximum

Three-State Fully Buffered Outputs

High Output Drive Capability

Independent Service Request Flip-Flop

Asynchronous Data Latch Clear

24 Pin DIP

PACKAGE CONFIGURATION

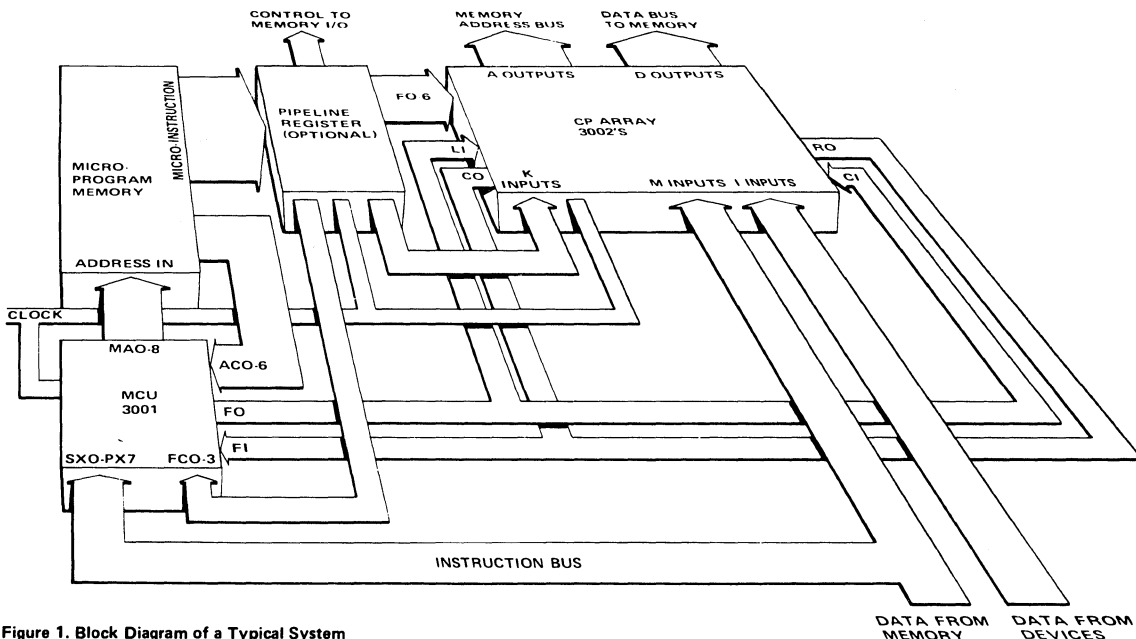
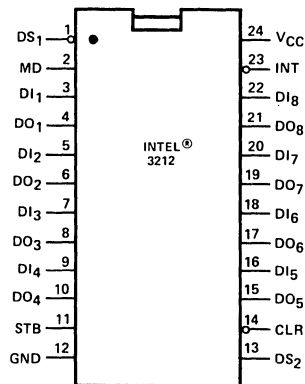


Figure 1. Block Diagram of a Typical System

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE ⁽¹⁾
1	DS ₁	Device Select Input 1	active LOW
2	MD	Mode Input When MD is high (output mode) the output buffers are enabled and the write signal to the data latches is obtained from the device select logic. When MD is low (input mode) the output buffer state is determined by the device select logic and the write signal is obtained from the strobe (STB) input.	
3, 5, 7, 9, 16, 18, 20, 22	DI ₁ –DI ₈	Data Inputs The data inputs are connected to the D-inputs of the data latches.	
4, 6, 8, 10, 15, 17, 19, 21	DO ₁ –DO ₈	Data Outputs The data outputs are the buffered outputs of the eight data latches.	three-state
11	STB	Strobe Input When MD is in the LOW state, the STB input provides the clock input to the data latch.	
12	GND	Ground	
13	DS ₂	Device Select Input 2 When DS ₁ is low and DS ₂ is high, the device is selected.	
14	CLR	Clear	active LOW
23	INT	Interrupt Output The interrupt output will be active LOW (interrupting state) when either the service request flip-flop is low or the device is selected.	active LOW

NOTE:

(1) Active HIGH, unless otherwise specified.

The 3212 contains eight D-type data latches, eight three-state output buffers, a separate D-type service request flip-flop, and a flexible device select/mode control section.

The Q-output of each data latch will follow the data on its corresponding data input line (DI_1-DI_8) while its clock input is high. Data will be latched when the internal write line WR is brought low. The output of each data latch is connected to a three-state, non-inverting output buffer. The internal enable line EN is bussed to each buffer. When the EN is high, the buffers are enabled and the data in each latch is available on its corresponding data output line (DO_1-DO_8).

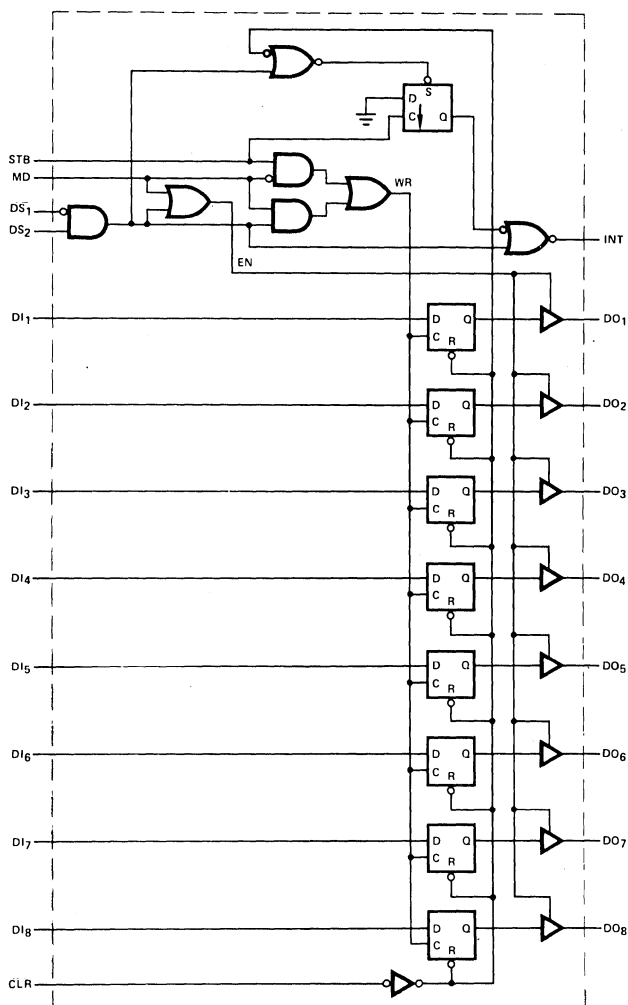
Two input lines DS₁ and DS₂ are provided for device selection. When DS₁ is low and DS₂ is high, the 3212 is selected.

The 3212 may be operated in two modes. When the mode input line MD is low, the device is in the input mode. In this mode, the output buffers are enabled whenever the 3212 is selected; the internal WR line follows the STB input line.

When MD is high, the device is in the output mode and, as a result, the output buffers are enabled. In this mode, the write signal for the data latch is obtained from the device select logic.

The service request flip-flop SR is used to generate and control central processor interrupt signals. For system reset, the SR flip-flop is placed in the non-interrupting state (i.e., SR is set) by bringing the CLR line low. This simultaneously clears (resets) the 8-bit data latch.

When operated in the input mode (i.e., MD low) the strobe input STB is used to synchronously write data into the data latch and place the SR flip-flop in the interrupting (reset) state. The interrupt is removed by the central processor when the interrupting 3212 is selected.



M3212 Logic Diagram

D.C. AND OPERATING CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	.0°C to 70°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = 0^\circ\text{C to } +75^\circ\text{C}$ $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_F	Input Load Current STB, DS ₂ , CLR, DI ₁ —DI ₈ Inputs			-.25	mA	$V_F = .45V$
I_F	Input Load Current MD Input			-.75	mA	$V_F = .45V$
I_F	Input Load Current DS ₁ Input			-1.0	mA	$V_F = .45V$
I_R	Input Leakage Current STB, DS, CLR, DI ₁ —DI ₈ Inputs			10	μA	$V_R = 5.25V$
I_R	Input Leakage Current MD Input			30	μA	$V_R = 5.25V$
I_R	Input Leakage Current DS ₁ Input			40	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			-1	V	$I_C = -5 \text{ mA}$
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	$I_{OL} = 15 \text{ mA}$
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1 \text{ mA}$
I_{SC}	Short Circuit Output Current	-15		-75	mA	$V_{CC} = 5.0V$
$ I_O $	Output Leakage Current High Impedance State			20	μA	$V_O = .45V/5.25V$
I_{CC}	Power Supply Current		90	130	mA	

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } 75^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PW}	Pulse Width	25			ns
t_{PD}	Data To Output Delay			30	ns
t_{WE}	Write Enable To Output Delay			40	ns
t_{SET}	Data Setup Time	15			ns
t_H	Data Hold Time	20			ns
t_R	Reset To Output Delay			40	ns
t_S	Set To Output Delay			30	ns
t_E	Output Enable Time			45	ns
t_C	Clear To Output Display			45	ns

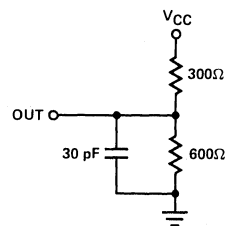
 $C_L = 30\text{ pf}$ **TEST CONDITIONS:**

Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5 ns between 1 volt and 2 volts.

Output load of 15 mA and 30 pF.

Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:**CAPACITANCE⁽¹⁾**

Symbol	Test	LIMITS			
		Min.	Typ.	Max.	Units
C_{IN}	DS ₁ , MD Input Capacitance		9	12	pf
C_{IN}	DS ₂ , CLR, STB, DI ₁ –DI ₈ Input Capacitance		5	9	pf
C_{OUT}	DO ₁ –DO ₈ Output Capacitance		8	12	pf

NOTE:

(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = -55^\circ\text{C to } +125^\circ\text{C}; V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_F	Input Load Current STB, DS ₂ , CLR, DI ₁ —DI ₈ Inputs			-.25	mA	$V_F = .45\text{V}$
I_F	Input Load Current MD Input			-.75	mA	$V_F = .45\text{V}$
I_F	Input Load Current DS ₁ Input			-1.0	mA	$V_F = .45\text{V}$
I_R	Input Leakage Current STB, DS, CLR, DI ₁ —DI ₈ Inputs			10	μA	$V_R = 5.5\text{V}$
I_R	Input Leakage Current MD Input			30	μA	$V_R = 5.5\text{V}$
I_R	Input Leakage Current DS ₁ Input			40	μA	$V_R = 5.5\text{V}$
V_C	Input Forward Voltage Clamp			1.2	V	$I_C = -5\text{ mA}$
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output "High" Voltage	3.5	4.0		V	$I_{OH} = .5\text{ mA}$
I_{SC}	Short Circuit Output Current	-15		-75	mA	$V_{CC} = 5.0\text{V}$
$ I_O $	Output Leakage Current High Impedance State			20	μA	$V_O = .45\text{V}/5.5\text{V}$
I_{CC}	Power Supply Current		90	145	mA	

A.C. CHARACTERISTICS $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PW}	Pulse Width	40			ns
t_{PD}	Data To Output Delay			30	ns
t_{WE}	Write Enable To Output Delay			50	ns
t_{SET}	Data Setup Time	20			ns
t_H	Data Hold Time	30			ns
t_R	Reset To Output Delay			55	ns
t_S	Set To Output Delay			35	ns
t_E	Output Enable Time			50	ns
t_C	Clear To Output Display			55	ns

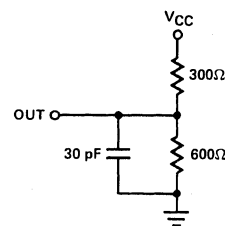
 $C_L = 30\text{ pf}$ **TEST CONDITIONS:**

Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5 ns between 1 volt and 2 volts.

Output load of 15 mA and 30 pF.

Speed measurements are taken at the 1.5 volt level.

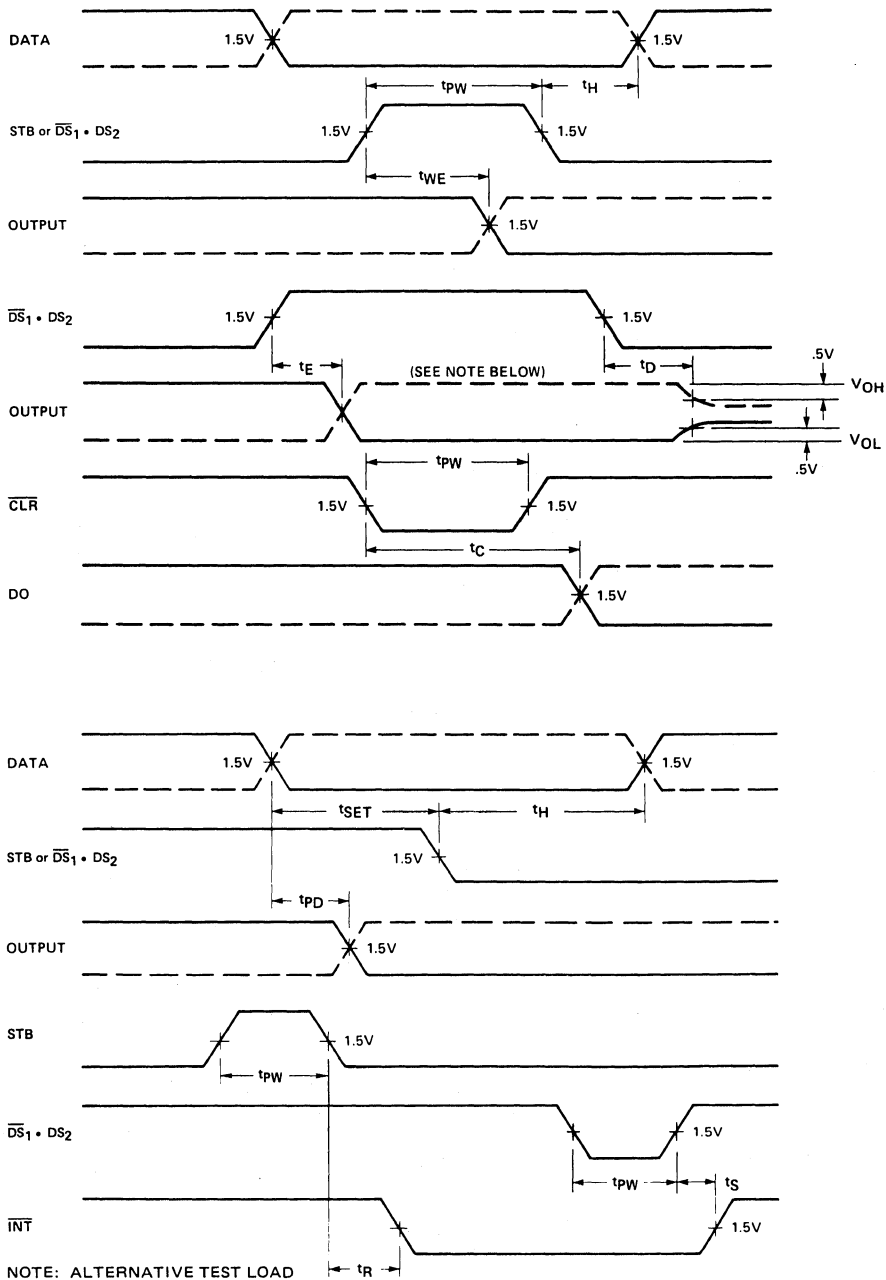
TEST LOAD CIRCUIT:**CAPACITANCE⁽¹⁾**

Symbol	Test	LIMITS			Units
		Min.	Typ.	Max.	
C_{IN}	DS ₁ , MD Input Capacitance		9	12	pf
C_{IN}	DS ₂ , CLR, STB, DI ₁ –DI ₈ Input Capacitance		5	9	pf
C_{OUT}	DO ₁ –DO ₈ Output Capacitance		8	12	pf

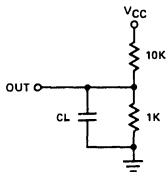
NOTE:

(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

WAVEFORMS



NOTE: ALTERNATIVE TEST LOAD



INTERRUPT CONTROL UNIT

The Intel®3214 Interrupt Control Unit (ICU) implements multi-level interrupt capability for systems designed with Series 3000 computing elements.

The ICU accepts an asynchronous interrupt strobe from the 3001 Microprogram Control Unit or a bit in microprogram memory and generates a synchronous interrupt acknowledge and an interrupt vector which may be directed to the MCU or CP Array to uniquely identify the interrupt source.

The ICU is fully expandable in 8-level increments and provides the following system capabilities:

Eight unique priority levels per ICU

Automatic Priority Determination

Programmable Status

N-level expansion capability

Automatic interrupt vector generation

High Performance – 80 ns Cycle Time

Compatible with Intel 3001 MCU and 3002 CPE

8-Bit Priority Interrupt Request Latch

4-Bit Priority Status Latch

3-Bit Priority Encoder with Open Collector Outputs

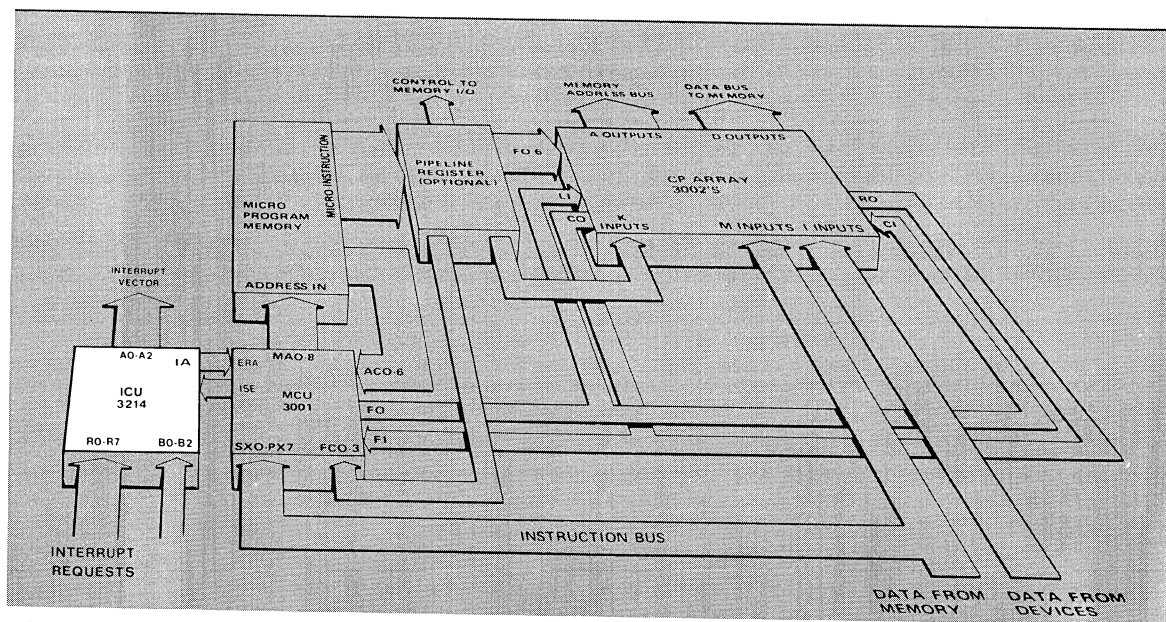
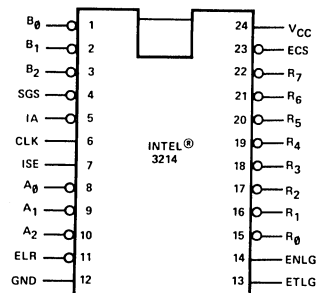
DTL and TTL Compatible

8-Level Priority Comparator

Fully Expandable

24-Pin DIP

PACKAGE CONFIGURATION



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE ⁽¹⁾
1–3	B ₀ –B ₂	Current Status Inputs The Current Status inputs carry the binary value modulo 8 of the current priority level to the current status latch.	Active LOW
4	SGS	Status Group Select Input The Status Group Select input informs the ICU that the current priority level does belong to the group level assigned to the ICU.	Active LOW
5	IA	Interrupt Acknowledge The Interrupt Acknowledge Output will only be active from the ICU (multi-ICU system) which has received a priority request at a level superior to the current status. It signals the controlled device (usually the processor) and the other ICUs OR-tied on the Interrupt Acknowledge line that an interrupt request has been recognized. The IA signal also sets the Interrupt Disable flip-flop (it overrides the clear function of the ECS input).	Active LOW Open-Collector Output
6	CLK	Clock Input The Clock input is used to synchronize the interrupt acknowledge with the operation of the device which it controls.	
7	ISE	Interrupt Strobe Enable Input The Interrupt Strobe Enable input informs the ICU that it is authorized to enter the interrupt mode.	
8–10	A ₀ –A ₂	Request Level Outputs When valid, the Request Level outputs carry the binary value (modulo 8) of the highest priority request present at the priority request inputs or stored in the priority request latch. The request level outputs can become active only with the ICU which has received the highest priority request with a level superior to the current status.	Active LOW Open-Collector
11	ELR	Enable Level Read Input When active, the Enable Level Read input enables the Request Level output buffers (A ₀ –A ₂).	Active LOW
12	GND	Ground	
13	ETLG	Enable This Level Group Input The Enable This Level Group input allows a higher priority ICU in multi-ICU systems to inhibit interrupts within the next lower priority ICU (and all the following ICUs).	
14	ENLG	Enable Next Level Group Output The Enable Next Level Group output allows the ICU to inhibit interrupts within the lower priority ICU in a multi-ICU system.	
15–22	R ₀ –R ₇	Priority Interrupt Request Inputs The Priority Interrupt Request inputs are the inputs of the priority Interrupt Request Latch. The lowest priority level interrupt request signal is attached to R ₀ and the highest is attached to R ₇ .	Active LOW
23	ECS	Enable Current Status Input The Enable Current Status input controls the current status latch and the clear function of the Interrupt Inhibit flip-flop.	Active LOW
24	V _{CC}	+5 Volt Supply	

NOTE:

(1) Active HIGH, unless otherwise noted.

FUNCTIONAL AND LOGICAL DESCRIPTION

The ICU adds interrupt capability to suitably microprogrammed processors or controllers. One or more of these units allows external signals called interrupt requests to cause the processor/controller to suspend execution of the active process, save its status, and initiate execution of a new task as requested by the interrupt signal.

It is customary to strobe the ICU at the end of each instruction execution. At that time, if an interrupt request is acknowledged by the ICU, the MCU is forced to follow the interrupt microprogram sequence.

Figure 1 shows the block diagram of the ICU. Interrupt requests pass through the interrupt request latch and priority encoder to the magnitude comparator. The output of the priority encoder is the binary equivalent of the highest active priority request. At the comparator, this value is compared with the Current Status (currently active priority level) contained in the current status latch. A request, if acknowledged at interrupt strobe time, will cause the interrupt flip-flop to enter the "interrupt active" state for one microinstruction cycle. This action causes the interrupt acknowledge (IA) signal to go low and sets the interrupt disable flip-flop.

The IA signal constitutes the interrupt command to the processor. It can directly force entry into the interrupt service routine as demonstrated in the appendix. As part of this routine, the microprogram normally reads the requesting level via the request level output bus. This information which is saved in the request latch can be enabled onto one of the processor input data buses using the enable level read input. Once the interrupt handler has determined the requesting level, it normally writes this level back into the current status register of the ICU. This action resets the interrupt disable flip-flop and acts to block any further request at this level or lower levels.

Entry into a macro level interrupt service routine may be vectored using the request level information to generate a subroutine address which corresponds to the level. Exit from such a macroprogram should normally restore the prior status in the current status latch.

The Enable This Level Group (ETLG) input and the Enable Next Level Group (ENLG) output can be used in a daisy chain fashion, as each ICU is capable of inhibiting interrupts from all of the following ICUs in a multiple ICU configuration.

The interrupt acknowledge flip-flop is set to the active LOW state on the rising edge of the clock when the following conditions are met:

An active request level (R_0-R_7) is greater than the current status B_0-B_2

The interrupt mode (ISE) is active
ETLG is enabled

The interrupt disable flip-flop is reset

When active, the IA signal asynchronously sets the disable flip-flop and holds the requests in the request latch until new current status information (B_0-B_2 , SGS) is enabled (ECS) into the current status latch. The disable flip-flop is reset at the completion of this load operation.

During this process, ENLG will be enabled only if the following conditions are met:

ETLG is enabled

The current status (SGS) does not belong to this level group

There is no active request at this level

The request level outputs A_0-A_2 and the IA output are open-collector to permit bussing of these lines in multi-ICU configuration.

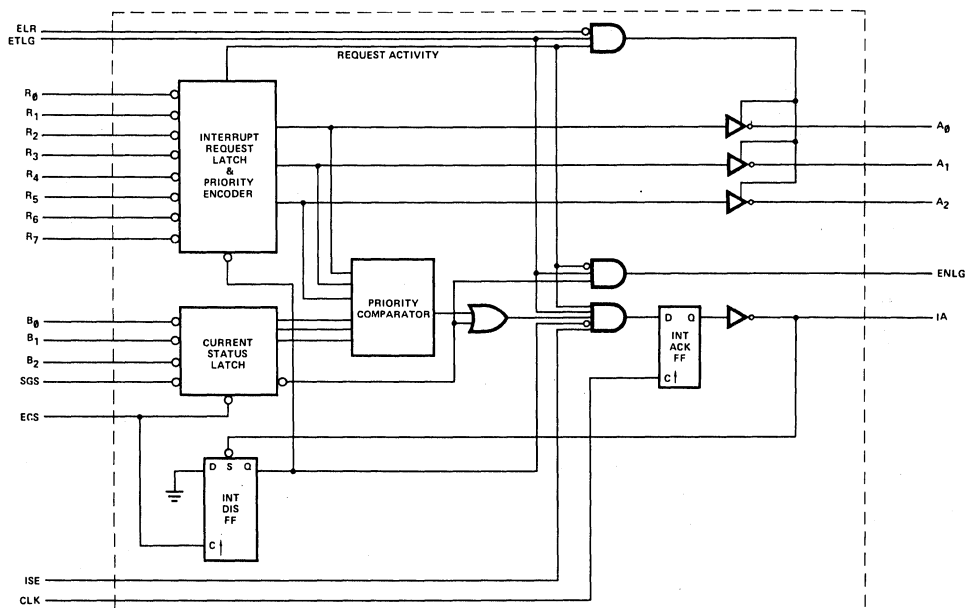


Figure 1. 3214 Block Diagram.

D.C. AND OPERATING CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	
Ceramic	-65°C to +75°C
Plastic	0°C to +75°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = 0^\circ\text{C to } +75^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

SYMBOL	PARAMETER		LIMITS			UNIT	CONDITIONS
			MIN	TYP ⁽¹⁾	MAX		
V _C	Input Clamp Voltage (all inputs)				-1.0	V	I _C = -5 mA
I _F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V _F = 0.45V
		all other inputs		-.08	-0.25	mA	
I _R	Input Reverse Current:	ETLG input			80	μA	V _R = 5.25V
		all other inputs			40	μA	
V _{IL}	Input LOW Voltage:	all inputs			0.8	V	V _{CC} = 5.0V
V _{IH}	Input HIGH Voltage:	all inputs	2.0			V	V _{CC} = 5.0V
I _{CC}	Power Supply Current ⁽²⁾			90	130	mA	
V _{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I _{OL} = 15 mA
V _{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I _{OH} = -1 mA
I _{OS}	Short Circuit Output Current: ENLG output		-20	-35	-55	mA	V _{CC} = 5.0V
I _{CEX}	Output Leakage Current:	IA and A ₀ -A ₂ outputs			100	μA	V _{CEX} = 5.25V

NOTES:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(2) B₀-B₂, SGS, CLK, R₀-R₄ grounded, all other inputs and all outputs open.

A.C: CHARACTERISTICS $T_A = 0^{\circ}\text{C to } +75^{\circ}\text{C}, V_{CC} = +5\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	LIMITS TYP ⁽¹⁾	MAX	UNIT
t_{CY}	CLK Cycle Time	80			ns
t_{PW}	CLK, ECS, IA Pulse Width	25	15		ns
<i>Interrupt Flip-Flop Next State Determination:</i>					
t_{ISS}	ISE Set-Up Time to CLK	16	12		ns
t_{ISH}	ISE Hold Time After CLK	20	10		ns
t_{ETCS}^2	ETLG Set-Up Time to CLK	25	12		ns
t_{ETCH}^2	ETLG Hold Time After CLK	20	10		ns
t_{ECCS}^3	ECS Set-Up Time to CLK (to clear interrupt inhibit prior to CLK)	80	25		ns
t_{ECCH}^3	ECS Hold Time After CLK (to hold interrupt inhibit)	0			ns
t_{ECRS}^3	ECS Set-Up Time to CLK (to enable new requests through the request latch)	110	70		ns
t_{ECRH}^3	ECS Hold Time After CLK (to hold requests in request latch)	0			ns
t_{ECSS}^2	ECS Set-Up Time to CLK (to enable new status through the status latch)	75	70		ns
t_{ECSH}^2	ECS Hold Time After CLK (to hold status in status latch)	0			ns
t_{DCS}^2	SGS and B ₀ -B ₂ Set-Up Time to CLK (current status latch enabled)	70	50		ns
t_{DCH}^2	SGS and B ₀ -B ₂ Hold Time After CLK (current status latch enabled)	0			ns
t_{RCS}^3	R ₀ -R ₇ Set-Up Time to CLK (request latch enabled)	90	55		ns
t_{RCH}^3	R ₀ -R ₇ Hold Time After CLK (request latch enabled)	0			ns
t_{ICS}	IA Set-Up Time to CLK (to set interrupt inhibit F.F. before CLK)	55	35		ns
t_{CI}	CLK to IA Propagation Delay		15	25	ns
<i>Contents of Request Latch and Request Level Output Status Determination:</i>					
t_{RIS}^4	R ₀ -R ₇ Set-Up Time to IA	10	0		ns
t_{RIH}^4	R ₀ -R ₇ Hold Time After IA	35	20		ns
t_{RA}	R ₀ -R ₇ to A ₀ -A ₂ Propagation Delay (request latch enabled)		80	100	ns
t_{ELA}	ELR to A ₀ -A ₂ Propagation Delay		40	55	ns
t_{ECA}	ECS to A ₀ -A ₂ Propagation Delay (to enable new requests through request latch)		100	120	ns
t_{ETA}	ETLG to A ₀ -A ₂ Propagation Delay		35	70	ns

A.C. CHARACTERISTICS (CON'T)

SYMBOL	PARAMETER	MIN	LIMITS TYP(1)	MAX	UNIT
<i>Contents of Current Priority Status Latch Determination:</i>					
t_{DECS}^4	SGS and B ₀ -B ₂ Set-Up Time to ECS	15	10		ns
t_{DECH}^4	SGS and B ₀ -B ₂ Hold Time After ECS	15	10		ns
<i>Enable Next Level Group Determination:</i>					
t_{REN}	R ₀ -R ₇ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	ECS to ENLG Propagation Delay (enabling new request through the request latch)		85	90	ns
t_{ECSN}	ECS to ENLG Propagation Delay (enabling new SGS through status latch)		35	55	ns

NOTES:

- (1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.
 (2) Required for proper operation if ISE is enabled during next clock pulse.
 (3) These times are not required for proper operation but for desired change in interrupt flip-flop.
 (4) Required for new request or status to be properly loaded.
 (5) $t_{CY} = t_{ICS} + t_{CI}$

TEST CONDITIONS:

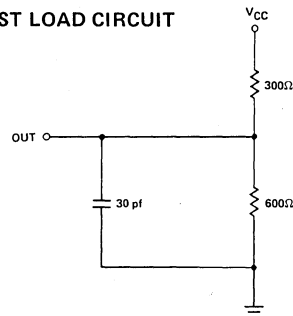
Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT

CAPACITANCE ⁽⁵⁾

$T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	LIMITS TYP(1)	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pf
C_{OUT}	Output Capacitance		7	12	pf

TEST CONDITIONS:

$V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$

NOTE:

- (5) This parameter is periodically sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	
CerDip	-55°C to +125°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C; V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER		MIN	LIMITS TYP(1)	MAX	UNIT	CONDITIONS
V _C	Input Clamp Voltage (all inputs)				-1.2	V	I _C = -5 mA
I _F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V _F = 0.45V
		all other inputs		-.08	-0.25	mA	
I _R	Input Reverse Current:	ETLG input			80	μA	V _R = 5.5V
		all other inputs			40	μA	
V _{IL}	Input LOW Voltage:	all inputs			0.8	V	V _{CC} = 5.0V
V _{IH}	Input HIGH Voltage:	all inputs	2.0			V	V _{CC} = 5.0V
I _{CC}	Power Supply Current(2)			90	130	mA	
V _{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I _{OL} = 10 mA
V _{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I _{OH} = -1 mA
I _{OS}	Short Circuit Output Current: ENLG output		-15	-35	-55	mA	V _{CC} = 5.0V
I _{CEX}	Output Leakage Current: IA and A ₀ -A ₃ outputs				100	μA	V _{CEX} = 5.5V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) B₀-B₂, SGS, CLK, R₀-R₄ grounded, all other inputs and all outputs open.

SERIES
3000

A.C. CHARACTERISTICS

 $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; $V_{CC} = 5.0\text{V} \pm 10\%$

SYMBOL	PARAMETER	MIN	LIMITS TYP ⁽¹⁾	MAX	UNIT
t_{CY}	CLK Cycle Time ⁽⁵⁾	85			ns
t_{PW}	CLK, ECS, IA Pulse Width	25	15		ns
<i>Interrupt Flip-Flop Next State Determination:</i>					
t_{ISS}	ISE Set-Up Time to CLK	16	12		ns
t_{ISH}	ISE Hold Time After CLK	20	10		ns
t_{ETCS}^2	ETLG Set-Up Time to CLK	25	12		ns
t_{ETCH}^2	ETLG Hold Time After CLK	20	10		ns
t_{ECCS}^3	ECS Set-Up Time to CLK (to clear interrupt inhibit prior to CLK)	85	25		ns
t_{ECCH}^3	ECS Hold Time After CLK (to hold interrupt inhibit)	0			ns
t_{ECRS}^3	ECS Set-Up Time to CLK (to enable new requests through the request latch)	110	70		ns
t_{ECRH}^3	ECS Hold Time After CLK (to hold requests in request latch)	0			ns
t_{ECSS}^2	ECS Set-Up Time to CLK (to enable new status through the status latch)	85	70		ns
t_{ECSH}^2	ECS Hold Time After CLK (to hold status in status latch)	0			ns
t_{DCS}^2	SGS and B_0 - B_2 Set-Up Time to CLK (current status latch enabled)	90	50		ns
t_{DCH}^2	SGS and B_0 - B_2 Hold Time After CLK (current status latch enabled)	0			ns
t_{RCS}^3	R_0 - R_7 Set-Up Time to CLK (request latch enabled)	100	55		ns
t_{RCH}^3	R_0 - R_7 Hold Time After CLK (request latch enabled)	0			ns
t_{ICS}	IA Set-Up Time to CLK (to set interrupt inhibit F.F. before CLK)	55	35		ns
t_{CI}	CLK to IA Propagation Delay		15	30	ns
<i>Contents of Request Latch and Request Level Output Status Determination:</i>					
t_{RIS}^4	R_0 - R_7 Set-Up Time to IA	10	0		ns
t_{RIH}^4	R_0 - R_7 Hold Time After IA	35	20		ns
t_{RA}	R_0 - R_7 to A_0 - A_2 Propagation Delay (request latch enabled)		80	100	ns
t_{ELA}	ELR to A_0 - A_2 Propagation Delay		40	55	ns
t_{ECA}	ECS to A_0 - A_2 Propagation Delay (to enable new requests through request latch)		100	130	ns
t_{ETA}	ETLG to A_0 - A_2 Propagation Delay		35	70	ns

A.C. CHARACTERISTICS (CON'T)

SYMBOL	PARAMETER	MIN	LIMITS TYP(1)	MAX	UNIT
<i>Contents of Current Priority Status Latch Determination:</i>					
t_{DECS}^4	SGS and B_0 - B_2 Set-Up Time to ECS	20	10		ns
t_{DECH}^4	SGS and B_0 - B_2 Hold Time After ECS	20	10		ns
<i>Enable Next Level Group Determination:</i>					
t_{REN}	R_0 - R_7 to ENLG Propagation Delay		45	70	ns
t_{TEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	ECS to ENLG Propagation Delay (enabling new request through the request latch)		85	110	ns
t_{ECSN}	ECS to ENLG Propagation Delay (enabling new SGS through status latch)		35	55	ns

NOTES:

- (1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.
 (2) Required for proper operation if ISE is enabled during next clock pulse.
 (3) These times are not required for proper operation but for desired change in interrupt flip-flop.
 (4) Required for new request or status to be properly loaded.
 (5) $t_{CY} = t_{ICS} + t_{CI}$

TEST CONDITIONS:

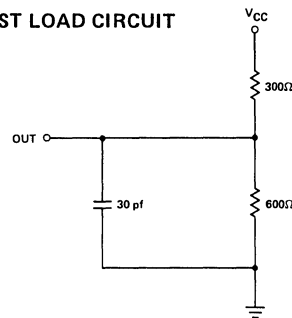
Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT

CAPACITANCE⁽⁵⁾

$T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	LIMITS TYP(1)	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pf
C_{OUT}	Output Capacitance		7	12	pf

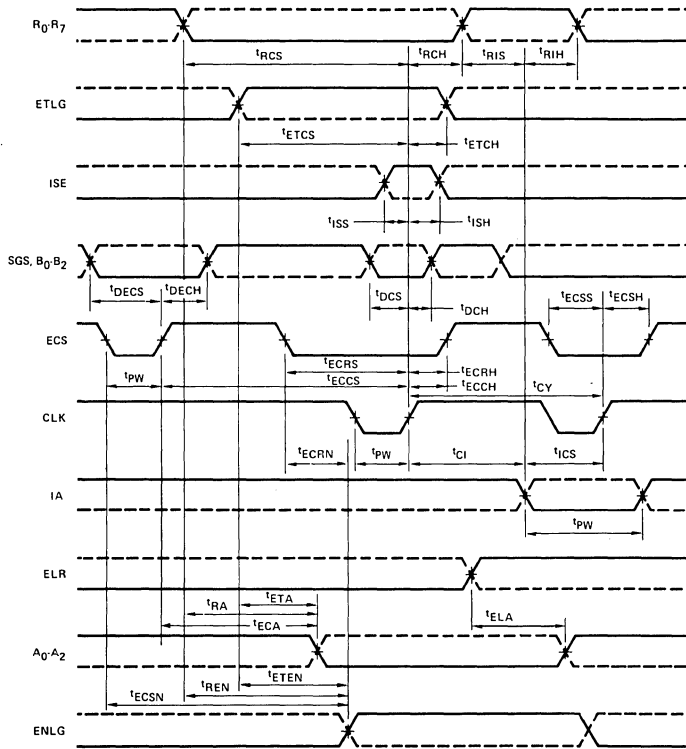
TEST CONDITIONS:

$V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$

NOTE:

- (5) This parameter is periodically sampled and not 100% tested.

WAVEFORMS





3216/3226

PARALLEL BIDIRECTIONAL BUS DRIVER

The INTEL® 3216 is a high-speed 4-bit Parallel, Bidirectional Bus Driver. Its three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems

The INTEL 3226 is a high-speed 4-bit Parallel, Inverting Bidirectional Bus Driver. Its three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems.

The 3216/3226 driver and receiver gates have three state outputs with PNP inputs. When the drivers or receivers are tri-stated the inputs are disabled, presenting a low current load, typically less than 40 μ amps, to the system bus structure.

High Performance—25 ns typical propagation delay

Low Input Load Current—0.25 mA maximum

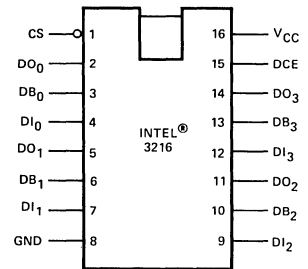
High Output Drive Capability for Driving System Data Busses

Three-State Outputs

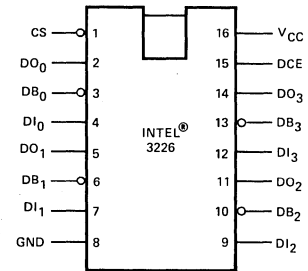
TTL Compatible

16-pin DIP

PACKAGE CONFIGURATION

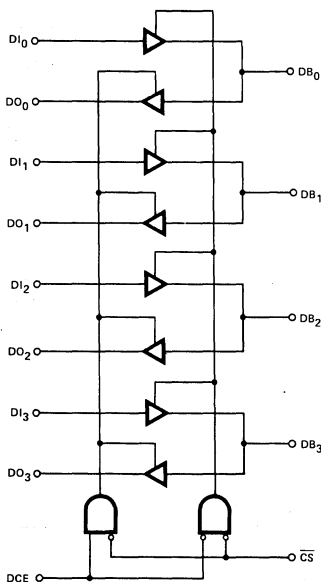


3216

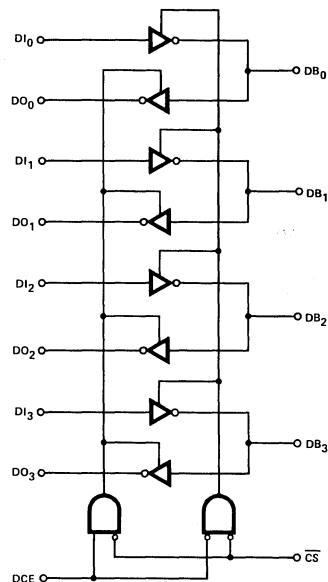


3226

LOGIC DIAGRAM 3216



LOGIC DIAGRAM 3226



SERIES
3000

D.C. AND OPERATING CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias

Ceramic -65°C to +75°C

Plastic 0°C to +75°C

Storage Temperature -65°C to +160°C

All Output and Supply Voltages -0.5V to +7V

All Input Voltages -1.0V to +5.5V

Output Currents 125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

 $T_A = 0^\circ\text{C to } +75^\circ\text{C}, V_{CC} = +5.0\text{V} \pm 5\%$

Symbol	Parameter	Min.	Limit Typ.	Max.	Unit	Condition
I_F	Input Load Current					
	DCE, CS Inputs		-0.15	-0.5	mA	$V_F = 0.45\text{V}$
	All Other Inputs		-0.08	-0.25	mA	
I_R	Input Leakage Current					
	DCE, CS Inputs			80	μA	$V_R = 5.25\text{V}$
	DI Inputs			40	μA	
V_C	Input Clamp Voltage			-1	V	$I_C = -5\text{mA}$
V_{IL}	Input Low Voltage			0.95	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.0			V	$V_{CC} = 5.0\text{V}$
V_{OL1}	Output Low Voltage DO, DB Outputs		0.3	0.45	V	DO Outputs $I_{OL} = 15\text{mA}$ DB Outputs $I_{OL} = 25\text{mA}$
V_{OL2}	Output Low Voltage DB Outputs Only		0.5	0.6	V	DB Outputs $I_{OL} = 50\text{mA}$
V_{OH1}	Output High Voltage DO Outputs Only	3.65	4.0		V	$I_{OH} = -1\text{mA}$
V_{OH2}	Output High Voltage DB Outputs Only	2.4	3.0		V	$I_{OH} = -10\text{mA}$
I_{SC}	Output Short Circuit Current					
	DO Outputs	-15	-35	-65	mA	$V_{CC} = 5.0\text{V}$
	DB Outputs	-30	-75	-120	mA	
$ I_O $	Output Leakage Current High Impedance State					
	DO Outputs			20	μA	$V_O = 0.45\text{V}/5.25\text{V}$
	DB Outputs			100	μA	
I_{CC}	Power Supply Current	3216	95	130	mA	
		3226	85	120	mA	

NOTE: Typical values are for $T_A = 25^\circ\text{C}$

3216, 3226

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } +75^\circ\text{C}, V_{CC} = +5.0\text{V} \pm 5\%$

Symbol	Parameter	Min.	Limit Typ.	Max.	Unit	Condition
T_{PD1}	Input to Output Delay DO Outputs	3216 3226	15 14	25 25	ns	$C_L = 30\text{pF}, R_1 = 300\Omega,$ $R_2 = 600\Omega$
T_{PD2}	Input to Output Delay DB Outputs	3216 3226	19 16	30 25	ns	$C_L = 300\text{pF}, R_1 = 90\Omega,$ $R_2 = 180\Omega$
T_E	Output Enable Time DCE, CS	3216 3226	42 36	65 54	ns ⁽²⁾	DO Outputs: $C_L = 30\text{pF},$ $R_1 = 300\Omega/10\text{K}\Omega,$ $R_2 = 600\Omega/1\text{K}\Omega$ DB Outputs: $C_L = 300\text{pF},$ $R_1 = 90\Omega/10\text{K}\Omega,$ $R_2 = 180\Omega/1\text{K}\Omega$
T_D	Output Disable Time DCE, CS		16	35	ns ⁽²⁾	DO Outputs: $C_L = 5\text{pF},$ $R_1 = 300\Omega/10\text{K}\Omega,$ $R_2 = 600\Omega/1\text{K}\Omega$ DB Outputs: $C_L = 5\text{pF},$ $R_1 = 90\Omega/10\text{K}\Omega,$ $R_2 = 180\Omega/1\text{K}\Omega$

NOTE: (1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(2) The test load circuit is set for worst case source and sink loading on the outputs. The two resistor values for R1 and R2 correspond to worst case sink and source loading, respectively.

CAPACITANCE⁽²⁾ $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limit			Unit
		Min.	Typ.	Max.	
C_{IN}	Input Capacitance	4	6		pF
C_{OUT}	Output Capacitance				
	DO Outputs	6	10		pF
	DB Outputs	13	18		pF

Note:

(2) This parameter is periodically sampled and is not 100% tested.

Condition of measurement is $f = 1\text{MHz}, V_{BIAS} = 2.5\text{V},$
 $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}.$

TEST CONDITIONS:

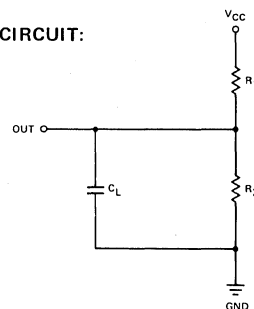
Input pulse amplitude of 2.5V.

Input rise and fall times of 5 ns between 1 and 2 volts.

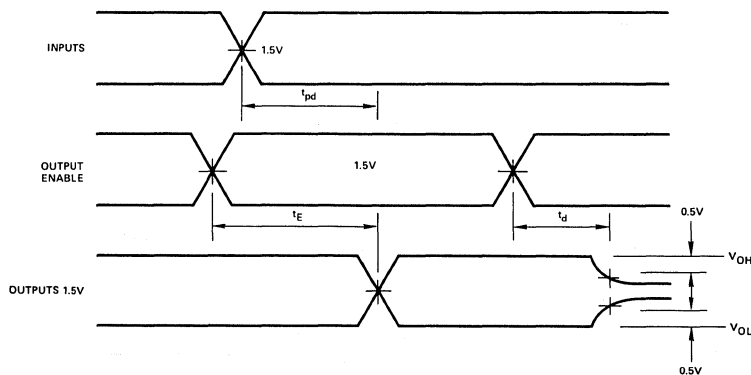
Output loading is 5 mA and 10 pF.

Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



WAVEFORMS



M3216, M3226

MILITARY TEMP.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias

Ceramic -65°C to +75°C

Storage Temperature -65°C to +160°C

All Output and Supply Voltages -0.5V to +7V

All Input Voltages -1.0V to +5.5V

Output Currents 125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm 10\%$

Symbol	Parameter	Min.	Limit Typ.	Max.	Unit	Condition
I_F	Input Load Current					
	DCE, \overline{CS} Inputs		-0.15	-0.5	mA	$V_F = 0.45\text{V}$
	All Other Inputs		-0.08	-0.25	mA	
I_R	Input Leakage Current					
	DCE, \overline{CS} Inputs			80	μA	$V_R = 5.5\text{V}$
	DI Inputs			40	μA	
V_C	Input Clamp Voltage			-1.2	V	$I_C = -5\text{mA}$
V_{IL}	Input Low Voltage	M3216 M3226		0.95	V	$V_{CC} = 5.0\text{V}$
				0.90	V	
V_{IH}	Input High Voltage	2.0			V	$V_{CC} = 5.0\text{V}$
V_{OL1}	Output Low Voltage DO, DB Outputs		0.3	0.45	V	DO Outputs $I_{OL} = 15\text{mA}$ DB Outputs $I_{OL} = 25\text{mA}$
			0.5	0.6	V	DB Outputs $I_{OL} = 45\text{mA}$
V_{OH1}	Output High Voltage DO Outputs Only	3.4	3.8		V	$I_{OH} = -0.5\text{mA}$ $I_{OH} = -2.0\text{mA}$
		2.4	3.0		V	$I_{OH} = -5\text{mA}$
I_{SC}	Output Short Circuit Current					
	DO Outputs	-15	-35	-65	mA	$V_{CC} = 5.0\text{V}$
	DB Outputs	-30	-75	-120	mA	
$ I_O $	Output Leakage Current					
	High Impedance State					
	DO Outputs			20	μA	$V_O = 0.45\text{V}/5.5\text{V}$
I_{CC}	Power Supply Current	M3216 M3226	95	130	mA	
			85	120	mA	

NOTE: Typical values are for $T_A = 25^\circ\text{C}$

SERIES
3000

M3216, M3226

MILITARY TEMP.

A.C. CHARACTERISTICS $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Min.	Limit Typ.	Max.	Unit	Condition
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	$C_L = 30\text{pF}$, $R_1 = 300\Omega$, $R_2 = 600\Omega$
T_{PD2}	Input to Output Delay DB Outputs	M3216 M3226	19 16	33 25	ns	$C_L = 300\text{pF}$, $R_1 = 90\Omega$, $R_2 = 180\Omega$
T_E	Output Enable Time	M3216 M3226	42 36	75 62	ns ⁽²⁾	DO Outputs: $C_L = 30\text{pF}$, $R_1 = 300\Omega/10\text{K}\Omega$, $R_2 = 600\Omega/1\text{K}\Omega$ DB Outputs: $C_L = 300\text{pF}$, $R_1 = 90\Omega/10\text{K}\Omega$, $R_2 = 180\Omega/1\text{K}\Omega$
T_D	Output Disable Time	M3216 M3226	16 16	40 38	ns ⁽²⁾	DO Outputs: $C_L = 5\text{pF}$, $R_1 = 300\Omega/10\text{K}\Omega$, $R_2 = 600\Omega/1\text{K}\Omega$ DB Outputs: $C_L = 5\text{pF}$, $R_1 = 90\Omega/10\text{K}\Omega$, $R_2 = 180\Omega/1\text{K}\Omega$

NOTE: (1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(2) The test load circuit is set for worst case source and sink loading on the outputs. The two resistor values for R_1 and R_2 correspond to worst case sink and source loading, respectively.

CAPACITANCE⁽²⁾ $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limit		Unit
		Min.	Typ.	
C_{IN}	Input Capacitance	4	6	pF
C_{OUT}	Output Capacitance			
	DO Outputs	6	10	pF
	DB Outputs	13	18	pF

Note:

(2) This parameter is periodically sampled and is not 100% tested.

Condition of measurement is $f = 1\text{MHz}$, $V_{BIAS} = 2.5\text{V}$,
 $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.

TEST CONDITIONS:

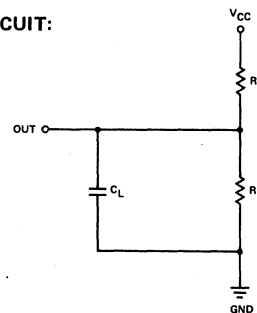
Input pulse amplitude of 2.5V.

Input rise and fall times of 5 ns between 1 and 2 volts.

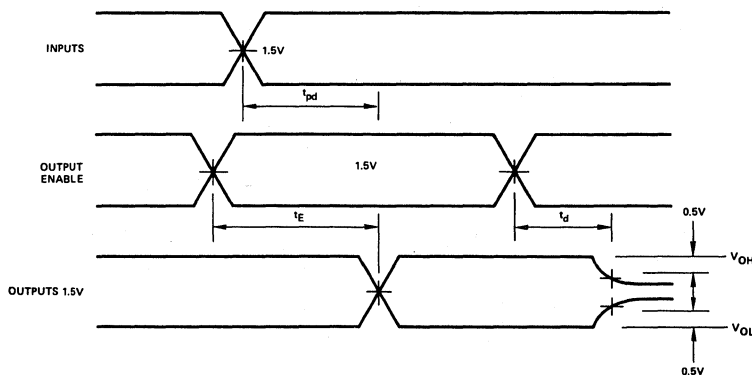
Output loading is 5 mA and 10 pF.

Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



WAVEFORMS



WF-3000 BIPOLAR SYSTEM DEVELOPMENT SET

The Intel WF-3000 Bipolar System Development Set contains the following members of the Schottky Bipolar LSI Microcomputer Set:

- (2) 3001 Microprogram Control Units
- (10) 3002 Central Processing Elements
- (10) 3601 Bipolar PROMs (256 x 4)

Includes all Computing Elements and High Speed Memory required for the construction of 16, 18, or 20 bit processors and/or High Speed Controllers.

N-Bit Word Expandable.

Multi-bus Organization.

High Performance

MCU Cycle Time — 700ns

CPE Cycle Time — 100ns

Total System Cycle Time — 150ns*

*Guaranteed worst case system cycle time for a 16-bit processor with a fast carry (3003) CP array, 3601-1 PROM Memory and a pipelined architecture.

A unique technology updating program insures that all set owners are kept abreast of Bipolar Microcomputer Set developments. This service includes priority mailings of additional design aids — application notes, specification sheets, user manuals — and free samples of new family members.

Upon receipt of the Bipolar system Development Registration Card, free samples of the following computing elements will be sent to development set owners:

3003 Look-Ahead Carry Generator

3212 Multi-Mode Latch Buffer

3214 Interrupt Control Unit

3226 Inverting Bi-Directional Bus Driver

In addition, free samples of new computing elements will be provided as they are announced throughout 1975.



ICE-30™ 3001 MCU IN-CIRCUIT EMULATOR

Extends the Inteltec® diagnostic capabilities into user configured systems, allowing in-circuit emulation of the user system's 3001 MCU

Direct Inteltec® System connection to the user configured system is achieved via an external cable with 3001 compatible 40-pin connector

Provides for the display of all 3001 address, status, and control lines for the current micro-instruction executed.

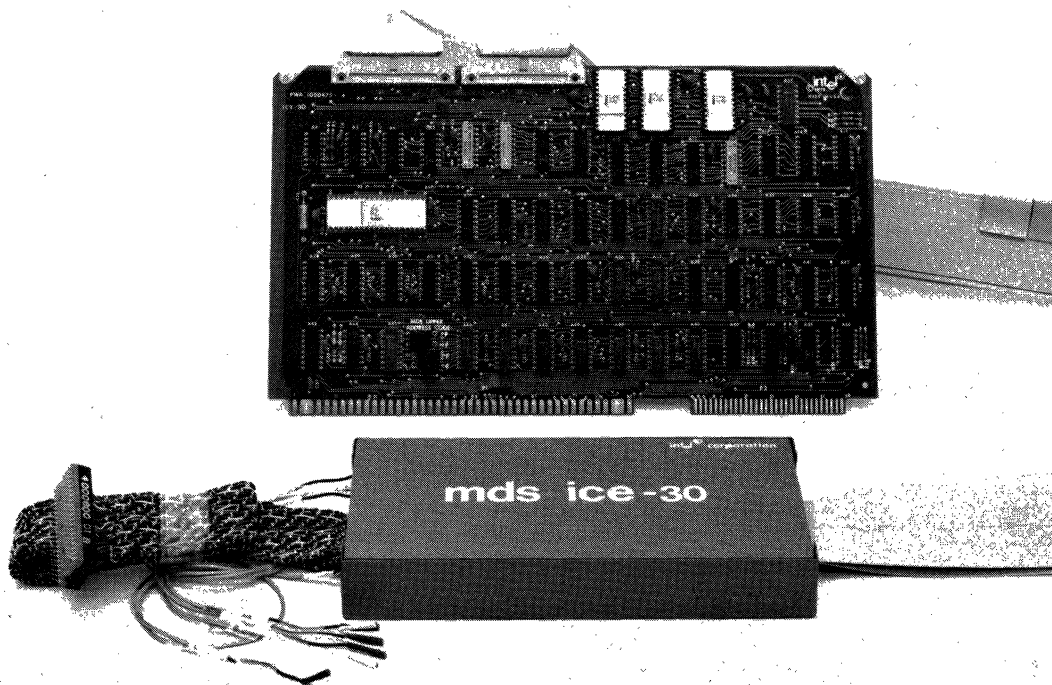
Allows for single-step microprogram execution

Presets the 9-bit 3001 Microprogram Address Register and sets two independent breakpoints on micro-instruction addresses generated by the 3001

Allows two independent breakpoints to be set on the logical combination of any three TTL compatible signals in the user system via three logic probes

Allows the microprogram word contents to be displayed and modified when used with the optional ROM-SIM modules

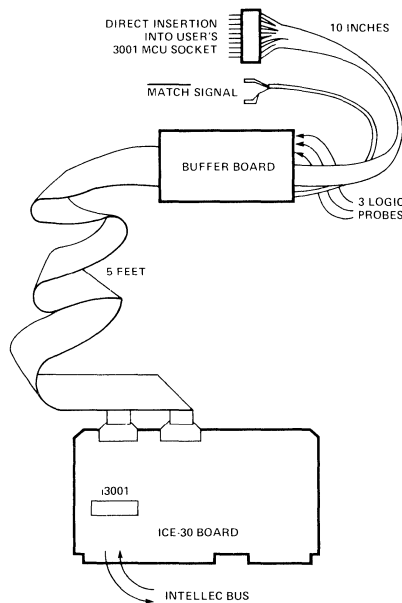
ICE-30 is an Inteltec resident module that provides the user with direct in-circuit emulation of the 3001 Microprogram Control Unit (MCU) and complete control over the execution of user developed microprograms. Through in-circuit emulation, the designer is able to set microprogram address breakpoints, single-step microprogram execution, and monitor all of the address, status, and control lines of the 3001.



HARDWARE

ICE-30 consists of a single PC board that resides in the Intellec System. An external cable from the board, terminating in a 3001 compatible 40-pin connector, forms the interface to the user system. Through the 3001 compatible connector, ICE-30 plugs directly into the user system's 3001 socket and allows the user to completely monitor and control all the activities of the MCU.

The figure below shows the hardware supplied with the ICE-30 package.



ICE-30 MODULE HARDWARE

By inserting the board into the Intellec Bus inside a basic Intellec system, a 3001 MCU chip in the user's system may be emulated. The ICE-30 board contains a 3001 MCU and peripheral logic required to monitor the 3001 operation and store trace information. The external cable carries status and control lines to and from the 3001 compatible 40-pin connector and the three logic probe lines. In addition, a MATCH line is brought out on the external cable which allows ICE-30 to control the user system's master clock and perform microprogram halt and single-step functions.

SOFTWARE

The ICE-30 Software Driver, ICE30SD, is an Intellec Microcomputer Development System RAM-resident program which provides a user interface with the ICE-30

hardware. ICE30 recognizes a set of commands issued by the user, translates the commands, and places the encoded results into a control block for the hardware. In this fashion, the user can establish a dialogue with the 3001 Microcomputer Control Unit (MCU) which is connected to the system, thus providing the capability to monitor, control or alter its operation.

ICE30 is capable of operating in conjunction with a RAM-based microprogram in the optional ROM-SIM modules (see ROM-SIM Data Sheet #98-211A). The commands provided by ICE30SD may therefore be divided into three categories: (1) Those commands unique to the optional ROM simulator, (2) Those which support ICE30SD functions, and (3) Those commands which are common to both ROM-SIM and ICE30SD.

ICE30 FUNCTION COMMANDS

SET	Assign values to the two hardware breakpoint registers, the 9-bit microprogram address register, and the PR latch.
GO	Initiates real-time emulation which continues until an address encountered matches one of the two breakpoint values.
STEP	Causes execution to proceed in a non-real-time single-step micro-instruction mode.
CONTINUE	Resumes step mode execution following a break condition.
ENABLE	Activates or deactivates the two hardware breakpoint registers prior to issuing the 'GO' command.
TRAP	Used to set or remove any of the five-step mode software traps (software breakpoint registers).

COMMON COMMANDS

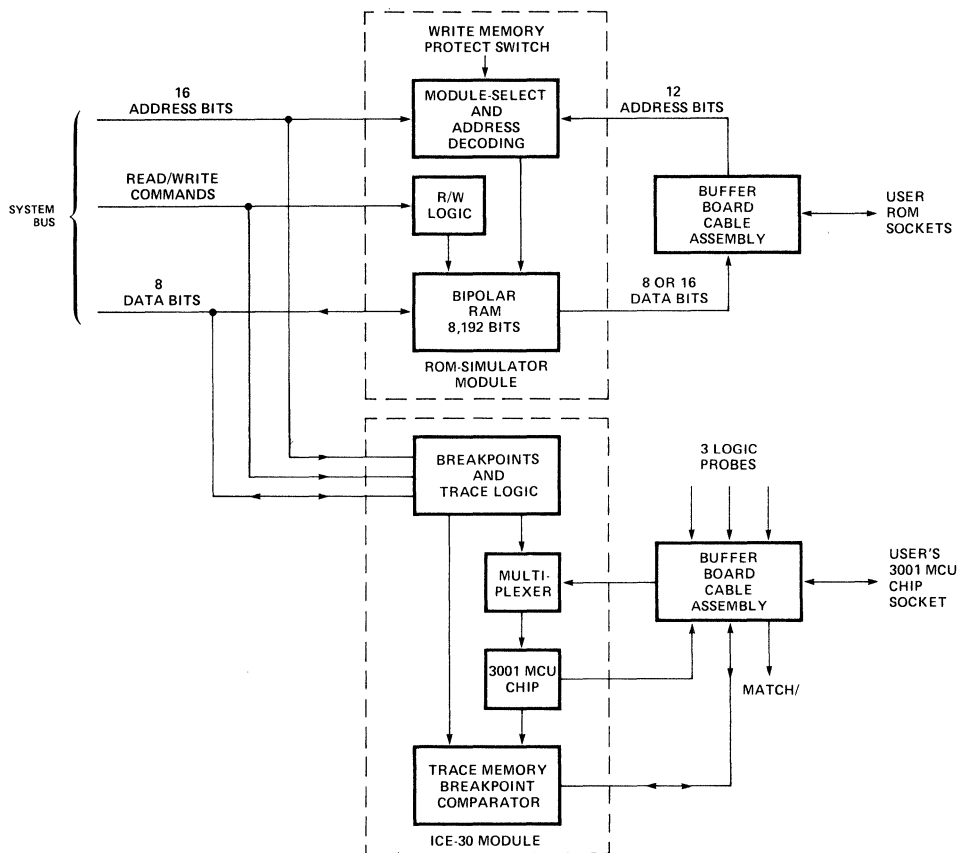
(Common to ICE30 and Optional ROM-SIM)

DISPLAY	Displays the contents of a specified address or address range in the simulated control storage.
BASE	Establishes a mode of display of all output data for the 'DISPLAY' command.
RESTART	Reinitializes all program variables, except the ROM-SIM configuration values, and starts execution at the point following the ROM-SIM configuration sequence.
EXIT	Causes ICE30SD to terminate.

ROM-SIM COMMANDS

ICE30SD provides commands necessary to drive the optional Intellec microprogram control storage simulation module, ROM-SIM. For a description of ROM-SIM capabilities, ask for the ROM-SIM Data Sheet #98-211A.

ICE30SD is written in Intel's high-level programming language PL/M and will execute in the minimum 16K RAM Intellec configuration.



FUNCTIONAL BLOCK DIAGRAM OF ICE-30 MODULE,
OPERATING IN CONJUNCTION WITH
ROM-SIMULATOR MODULE

SPECIFICATIONS

PHYSICAL CHARACTERISTICS

(Printed Circuit Board)

Width: 12.00 in.

Height: 6.75 in.

Depth: 0.50 in.

EQUIPMENT SUPPLIED

Printed Circuit Board

Interface Cables and

Buffer Enclosure Assembly

Reference Manual

Software Paper Tape

ORDERING INFORMATION

Part Number	Description
MDS-30-ICE	3000 Series In-Circuit Emulator